service manual

SYNTEX

WELSON
WEBO ELECTRONICS CO. S.p.A.
60020 PASSATEMPO - ITALY

SYNTEX

PAGE 1

The Syntex is a musical instrument made up from an analogic part (VCF and VCA -POWER SUPPLY and ADSR) and from a digital part. SMALL KEYBOARD WITH MEMORY - CODE CONVERTOR - CONTROL BOARD AND OSC. 1 AND OSC. 2. -

For the functioning of the SYNTEX other than inserting some footages, the filter must also be opened (VCF) and the amplifier driven (VCA)

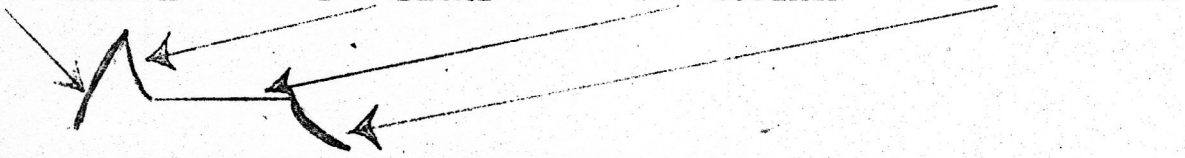
The commands to VCF and to VCA can be given in two ways:-

1) STATIC with the sending of continuous tension
2) DYNAMIC with the sending of a pulsating tension denominated ADSR.

The static command to VCF is done through the POT-FR, which, when in the position OFF sends to the filter - 12V. until it arrives at the position ON (all at high) with + 12V.
The static command to VCA is given through the push-button INITIAL VOLUME, which then sends +5V. to VCA.
With the VCF open and with the INITIAL VOLUME inserted the SYNTEX will always play and the intensity of sound can be regulated by the VOLUME potentiometer.

The dynamic command to VCF is given through the POT. AMOUNT ADSR. VCF, which regulates the level of pulsating tension to VCF.
The dynamic command to VCA is given through the POT. AMOUNT ADSR - VCA. With these commands the SYNTEX is able to simulate all of the instruments, since the dynamic command ADSR (which is made up of 4 wave lengths, namely:-

A = ATTACK D = DECAY S = SUSTAIN R = RELEASE



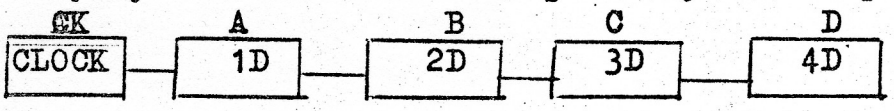
allows us to have an ATTACK, a DECAY and a SUSTAIN which regulates the level of sound, and a RELEASE for continuing a note for a certain length of time after the key has been released.)

DIGITAL PART OF THE SYNTEX

To be able to understand this part, the concept of the binary system must be introduced, the code and the function of the 4 basilary gates of the binary logic AND - NAND - OR and NOR.

BINARY SYSTEM OR ALGEBRA OF BOOL AND DEFINITION OF THE CODE

In the binary system 1 + 0 = 1 .
exists a relationship between the arab numbers and the binary system which can be explain by an example:-



The outputs of A of B of C and of D are called BIT
The togetherness of 30 plus BIT forma code.

The clock is an oscillator, the impulses of which, in time can be defined as a simple and pure counting in arab numbers:
0 - 1 - 2 - 3 - 4 - 5 - 6 - 7----------
Now we shall take a look at the 4 dividers in fall placed following the clock 1d - 2d - 3d - 4d, which, let us suppose, have a reset (initial take-off all from zero) and which state with the negative fronts to which can be constructed the Fig.A the consequence of which can be seen from the table herebelow:

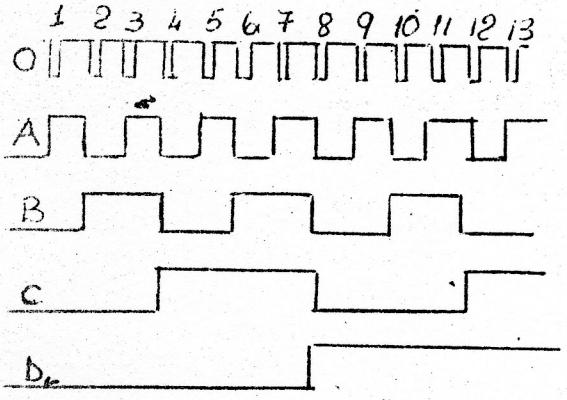


FIG. A.

$2^3=8$	$2^2=4$	$2^1=2$	$2^0=1$	
D	C	B	A	CK
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15
0	0	0	0	16

The information which gives the 4 dividers in time, are in close relation with the arab number of the CLOCK.
This can be deducted from FIG. A where you can also see how every divider changes its state with the negative fronts.
In the table beside FIG. A you can see how the BIT when put in fall, has the functions of 2, elevated from take-of until arrival 2^{γ} if γ are the bit.

To write a number in binary code, the state of the Bit must be taken into consideration; example:-
a) a1 number of clock corresponds to state 1 only in bit $2^0=1$.
b) a2 number of clock corresponds to state 1 only in bit $2^1=2$
c) a3 number of clock corresponds to state 1 only in bit $2^0=1$ and $2^1=2$ the sum of which is equal to 3
At number 4 of clock the state 1 corresponds in the bit $2^2=4$
At number 5 of clock the state 1 in the bit $2^0=1$ and $2^2=4$, the sum of which is equal to 5.
After all, to write a code in relation to the number of CLOCK, it is sufficient to do the sum of the interested BIT to make the construction of number, and put the state 1 in those Bit and the state 0 in the others.
Example: 6 in a code of 5 BIT and given the state 1 of the BIT 4 and 2 therefore:-

16 8 4 2 1
0 0 1 1 0 = 6

7 is given by state 1 of BIT 4 - 2 and 1 therefore:

16 8 4 2 1
0 0 1 1 1 = 7

8 is given by state 1 of BIT 8 therefore:

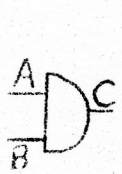
16 8 4 2 1
0 1 0 0 0 = 8

GATE INTEGRATED CIRCUITS

The integrated circuits TTL are supplied by 4,75 ÷ 5, 25 V.
The logic state 0 is included from 0 to 0, 80; the logic state 1 is included between 2,2 and 4,50 the level between 0,8V and 2,2V is not a logic state, and can therefore be considered as an error.

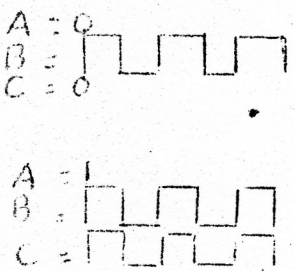
AND

The GATE AND makes the product of 2 functions and is supplied as follows



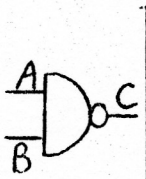
A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

As can be seen from the table of truth the 0 in an input A or B block the Output C to 0



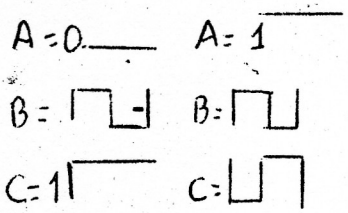
NAND

The GATE NAND makes the negative product of 2 functions and is screened as follows



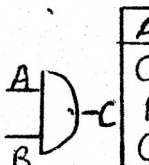
A	B	C
0	0	1
1	0	1
0	1	1
1	1	0

As can be seen from the table of truth the 0 in an input A or B block the Output C to 1



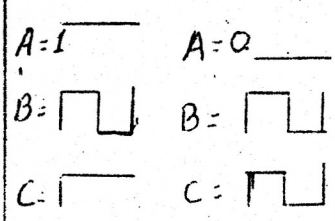
OR

The GATE OR does the sum of 2 functions and is screened as follows



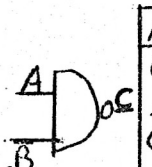
A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

As can be seen from the table of truth the state 1 in an input A or B block the output C to 1



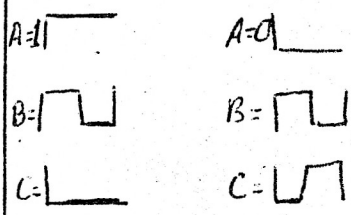
NOR

The Gate NOR does the negative sum of 2 functions and is screened as follows



A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

As can be seen from the table of truth the state 1 in an input A or B block the output C to 0



FORMATION OF THE NOTES IN THE SYNTEX

When a key is depressed a command is sent to the board SMALL KEYBOARD with MEMORY MOD. 216, which at its turn, sends out a code of 6 BIT in the old version and at 12 BIT in the new version. This code is then sent into the CODE CONVERTER board (Mod. 284 for the new version) and Mod. 226 and Mod. 217 (in the old version). The first circuit board Mod. 226 receives 4 BIT - ABCD of the 6BIT of TAST with M and sends out 10 BIT which should be controlled, at any time there is an error of note, only for the highest octave as this is repeated afterwards. The second circuit board Mod. 217, the E and F BIT from T with M + 10 BIT of circuit board MOD. 226. The BIT of the second circuit board Mod. 217 are to be controlled on all keys if an error in note should be found at any time.

The output of the CODE CONVERTER group Mod. 284 in the new version and Mod. 226 and Mod. 217 in the old version, are made up of 12 BIT., which are sent to the circuit board of control Mod. 229.
This circuit board Mod. 229 carries out 5 functions:-

1) Reading and direct output of CODE at 12 BIT
2) Manipulation of CODE at 12 BIT for the GLIDE effect
3) Music Random
4) Formation of an analogic tension relative to the CODE which is used for the GLIDE oscillator and to drive the VCF so as to make it in tune, for playing the whole keyboard.
5) Command for ADSR take-off.

When the GLIDE and the MUSIC RANDOM are not being used, the code comes directly out from Mod. 229 and is sent to Oscillator 1 and Oscillator 2 Mod. 223.
Oscillator 1 and Oscillator 2 are both different from each other for the frequency of oscillation; Osc. 1 = 1,8mhz. Osc. 2 = 3,2mhz. The code coming from Mod. 229, goes into the 3 programmed dividers (74191) which, depending on the code, divides for one number or another the frequency of the oscillator. The lowest number of division is 392 (which determines the highest note). This note becomes again divided by 4 dividers so as to obtain the 4 footages. To control a code of 12 BIT you must use a sheet of all of the codes which come out of the Code Converter Mod. 284 or from the last circuit board Mod. 217 in the first version, in relation to the key depressed. Also to control the output code of the KEYBOARD with MEMORY, you must use the sheet of codes herewith enclosed.

KEYBOARD WITH MEMORY MOD. 216

This circuit board is made up of:-

N.6	74151	MULTIPLEXER
N.1	74155	DECODER
N.2	7475	LATCH
N.1	7430	GATE AT 8 INPUTS
N.1	7413	SMITT TRIGGER
N.1	7410	TRIBLE GATE AT 2 INPUTS
N.1	7405	6-INVERTER OPEN COLLECTOR
N.1	74121	MONOSTABLE
N.2	7493	DIVIDERS

The multiplexers are TTL devices which have 8 inputs, which can be selected from a code at 3 BIT, this means that an

input corresponds to every code, which in correspondence to its code can go out in a direct manner, or refused by the respective outputs PIN 5, PIN 6, only if the PIN 7 is at a logic level 0.
The code is addressed in the PIN 11 = A, PIN 10 = B, PIN 9 = C:

4	2	1	
C	B	A	
0	0	0	RELATIVE INPUT PIN 4
0	0	1	" " " 3
0	1	0	" " " 2
0	1	1	" " " 1
1	0	0	" " " 15
1	0	1	" " " 14
1	1	0	" " " 13
1	1	1	" " " 12

DECODER 74155

The DECODER is a TTL, to which, by sending a code of 3 BIT you can obtain at its 8 outputs, a zero scale starting from the output relative to the CODE 000 until you have arrived at the output relative to CODE 111.. The code is addressed to the PIN 13 = A; PIN 3 = B and PIN 1 and 15 = C.

4	2	1	
C	B	A	
0	0	0	When this code arrives at PIN 9 it goes to 0 Logic
0	0	1	" " " " " 10 level
0	1	0	" " " " " 11
0	1	1	" " " " " 12
1	0	0	" " " " " 7
1	0	1	" " " " " 6
1	1	0	" " " " " 5
1	1	1	" " " " " 4

NAND GATE AT 8 INPUTS 7430

This gate has an output which is the inverted product of the 8 inputs.

SCHMITT TRIGGERED DOUBLE 7413

This has a thresh-hold of intervention which is about 1,7V and the two outputs invert the input levels.

DIVIDER 7493

This is a divider at 4 states. To divide, the Pin 2 and 3 must be at level 0, All of the outputs are reset at level 1.

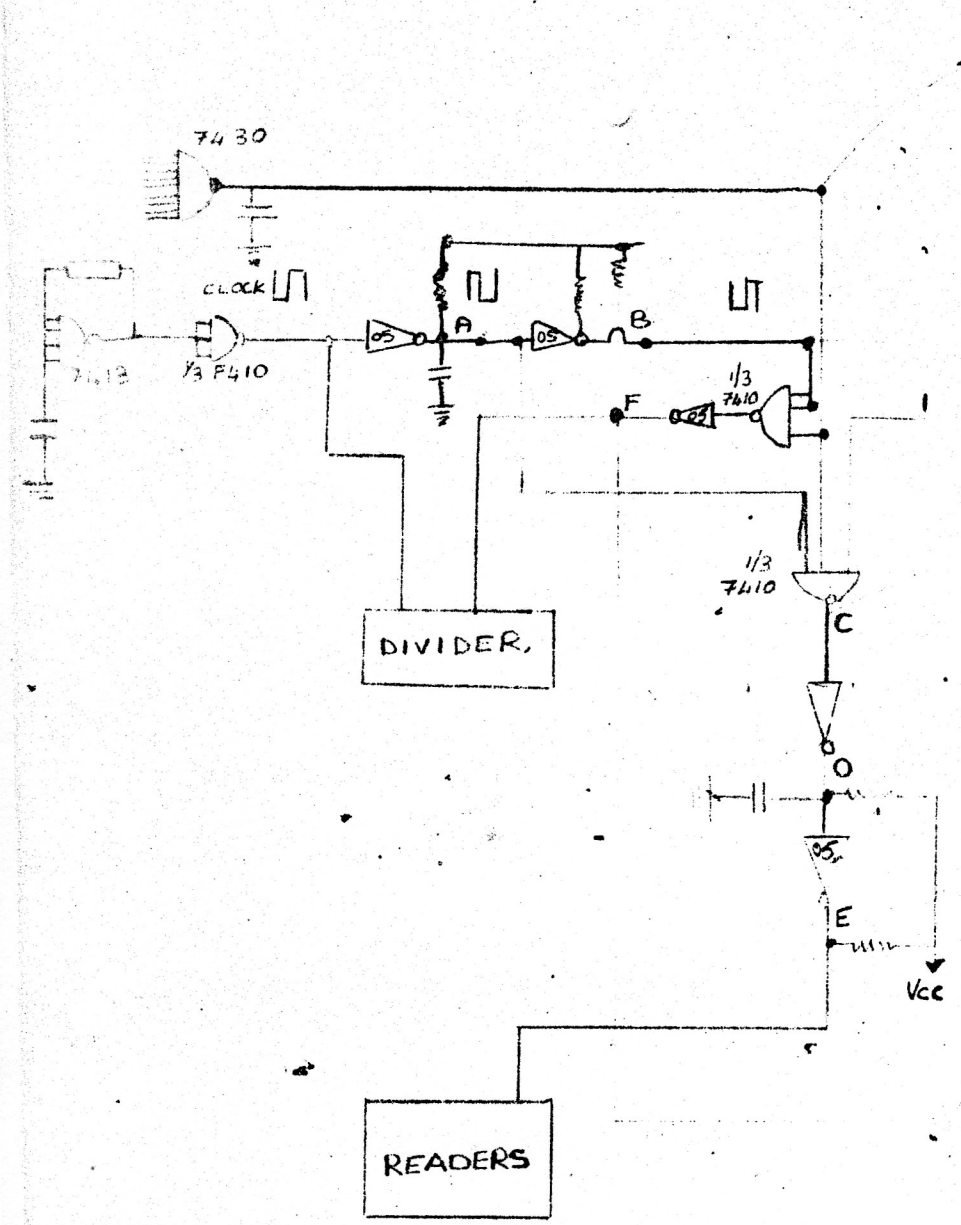
LATCH 7475

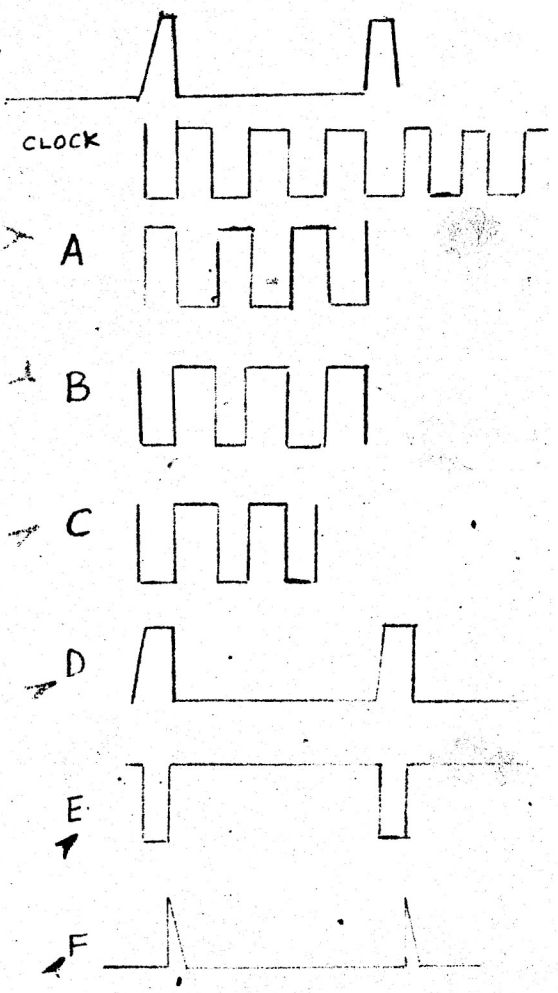
This is a two sectioned latch, and by connecting PIN 4 and 13 together, you can obtain the reading of a code at 4 BIT. The Clock must be positive. The code is present at inputs PIN 2 - 3 - 6 - 7. As soon as a positive impulse of clock arrives at Pin 4 and 13 the code is written in output of the outputs Pin - 16 - 15 - 10 - 9. The outputs $\bar{Q}$ Pin 1 - 14 11 - 8 give the code inverted.

The circuit board Mod. 216 has an oscillator made from one half of 7413 and this oscillates at 470 KHz. This oscillator or clock comes out from 7413 and is passed through a section of 7410 it then goes to pilot the divider 29722 - 74748BF - 74746BF for the circuit board made in the first manner, while in the latest circuit board version, it drives two 7493, placed in fall. In both cases the 6 dividers are exploited, the first 3 for sending the code to these 74151 and the last 3 for sending the code to 74155. The outputs of the 6 dividers also go to the readers 74193 X 2 first version and 7475 latest version, these 6 outputs can write a maximum of 64 codes at 6 Bit and the time employed to pass 64 beats of CLOCK is in the order of 130μsec. In the inputs of the 6-74151 , all the keys of the keyboard are connected, and when these are depressed they send logic levels 1 to the relative inputs.

After having turned on the instrument and without having touched any of the keys, you will have all the inputs of 74151 at 0, and therefore, all of their outputs PIN 6 to 1 which, being connected to the 8 inputs of 7430 will make at the outputs of these one 0, which is then sent in the two GATE at 3 inputs 1/3 7410, which at its turn, having an 0 in input gives 1 at the outputs.
The output of 1/3 7410, connected to an inverter, the output of which is connected to Pin 13 and 5 (RESET) of 29722, first version, and to Pin 2 and 3 of 7493 second version, being 1 puts 0 at the output of the inverter and therefore to the PIN of the RESET, a level which allows the divider to divide.
While the output C of 7410 1/3 is connected to an inverter, the output D of which is connected to another inverter, the output E of which is connected to Pin------ of 7475, bringing a level 0 which does not allow for the reading in output of the CODE of input.
Therefore, we have seen that without depressing the keys, the CLOCK oscillates, the divider divides, putting the codes at the disposal of the 74155 and of the 74193 or 7475, which however do not give a reading.

MOD. 216

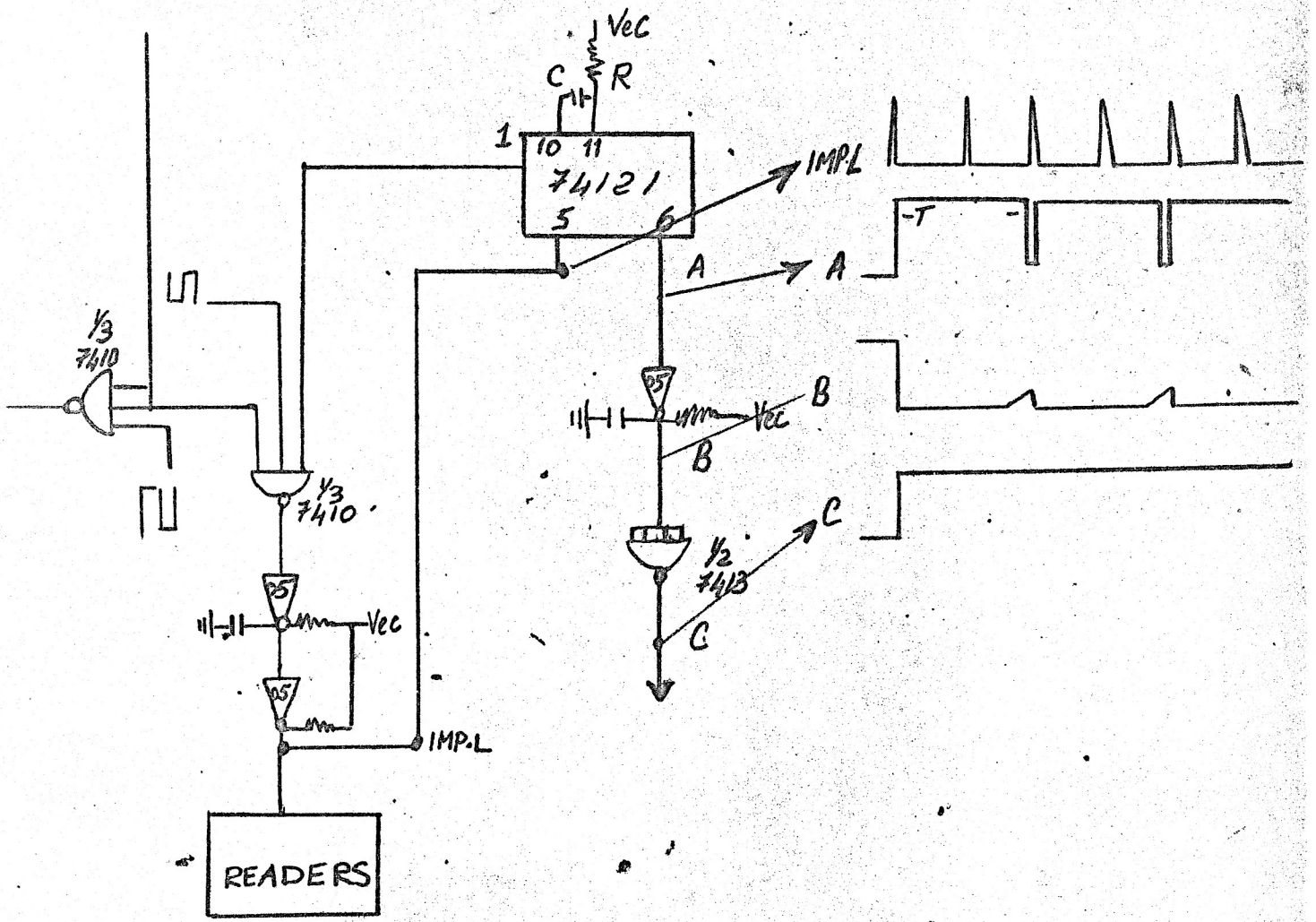

7430
CLOCK
1/3 7410
A
B
1/3 7410
F
DIVIDER
1/3 7410
C
D
E
Vcc
READERS


CLOCK
A
B
C
D
E
F

Now let us suppose that the highest DO of the small keyboard is depressed which sends a level 1 to Pin 1 of the first 74151 which, to come out of Pin 6, must have a code 011 this code which may not be ready, because on depressing the clock could have been at 30 and therefore you must wait until it arrives at 67, this delay which is very brief cannot be percepted by the ear, that is why the note seems to arrive immediately.
As soon as the 011 code arrives in piano 74151, given that in 74155 the code 000 is present, which allows for having 0 at the output Pin 9 and therefore 0 at Pin 7 of 74151; it has in its inverted output Pin 6 a level 0 which being connected to an input of 7430 allows for having level 1 at the output of these.

As can be seen from the designed wavelengths (relative to the various points of the circuit at the moment in which a key is depressed) the impulse at level 1 of 7430 arrives in a nearly total syncronism with negative front of CLOCK (it is not in perfect syncronism for the effect of the capacitor which is present at output of 7430).
This impulse allows for having at point C a negative impulse, and therefore, an impulse which is delayed and negative in point E, a point of command for the reading (output of code present at that instant in the input) of the READERS.
This comes about in the first half period of the CLOCK, while in the second half period there is an impulse of RESET, for the divider which puts all the codes at 0, therefore the impulse disappears (always with the key depressed), in the output of 7430 and when the clock and the divider starts again to form codes until arriving at 3 = 011, in our case 1 is made to come out of output of 7430 and always the same while the key is being held.
The impulse of reading must arrive before that of RESET to allow the readers to read.
The circuit designed here, is a circuit of delay which is used to avoid inconveniences such as mechanical jumps of the keys. This circuit is in fact formed from a monostable, the input of which is commanded by the same impulse which is used for the reading of the readers, the outputs of which (Pin 1 goes to command section 1/3 7410 which is used to give the impulse of reading and given that on arrival of the impulse the Pin 1 of 74121 is brought to level 0 for a time T = 0,7 R.C and therefore you have level 0 after the inverter and level 1 after ½ of 7413.

CIRCUIT OF DELAY



It is said, that the code coming out of T with M arrives at the CODE CONVERTER Circuit board which then converts this code

into another of 12 Bit.
The codes relating to every key are written on a sheet herewith enclosed, together with a diagram showing the different GATES which placed in that particular way, carry out that given function.

To repair this circuit board it is sufficient to follow the input levels for the various GATES until you arrive at the outputs.

CIRCUIT BOARD OF CONTROL MOD. 229

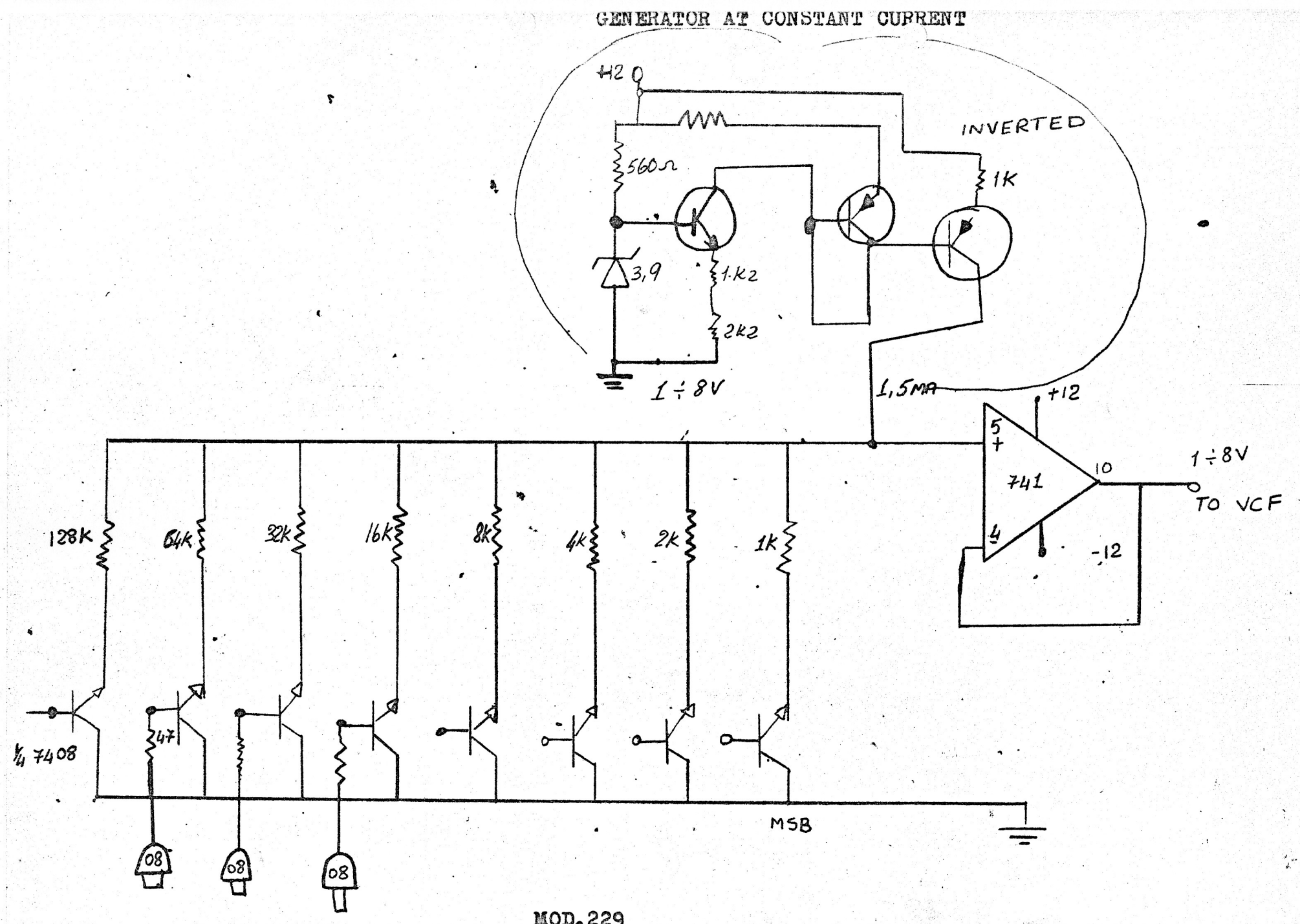
This circuit board is made up of:

N.3	74193	UP DOWN COUNTERS
N.3	9324	COMPARATORS OF LARGENESS
N.1	7451	NAND NAND NOR
N.1	7400	NAND
N.1	7405	INVERTOR
NK1	7472	DIVIDER
N.3	7408	AND

74193 are counters which can count upwards entering with the CLOCK in Pin 5 and downwards entering with the CLOCK in Pin 4 and they are also readers. The inputs are the Pins D C B A 9-10 -1-15 the outputs are pins D C B A 7-6-2-3 . To work as readers, they must have a level 0 in Pin 11, and in this condition the code at points 9-10-1-15 coming out directly at points 7-6-2-3.
When the Pin 11 is at level 1 they are counters and not readers. As counters they can go upwards from 0 to 15, arriving at 15, the output UP Pin 12 gives a negative impulse or counts downwards, this means, that it starts from 15 until it reaches 0, arriving at 0 the output DOWN Pin 13 gives a negative impulse. While counting the outputs D C B A 7-6-2-3 they move in fall as the dividers do.
The Pin 14 of these integrated circuits must be earthed.

9324 are comparators of measurement. (codes) this means that two codes can be put at 5 Bit called B and A in the respective inputs B4 B3 B2 B1 B0 and A4 A3 A2 A1 A0 the comparators 7 -6 -5 -4 -3 9 -10-11-12-13 indicate which of the two codes is minor, major or equal; in fact they have three outputs A > B = Pin 15; A < B = Pin 2; A = B Pin 14.

GENERATOR AT CONSTANT CURRENT



MOD. 229

CODE CONVERTER

The outputs give the indications with a level 1

example:

A > B	the output	A > B = 1	A < B = 0	A = B = 0
A < B	" "	A < B = 1	A > B = 0	A = B = 0
A = B	" "	A = B = 1	A > B = 0	A < B = 0

Out of the 5 functions of this circuit board, we shall examine that of the direct reading of the code; this means that it is not put in GLIDE, or MR, therefore, the Pin 8 of 7400 is at a level 0, because both MR and GLIDE ON (Pin 9 and Pin 10) are at level 1.

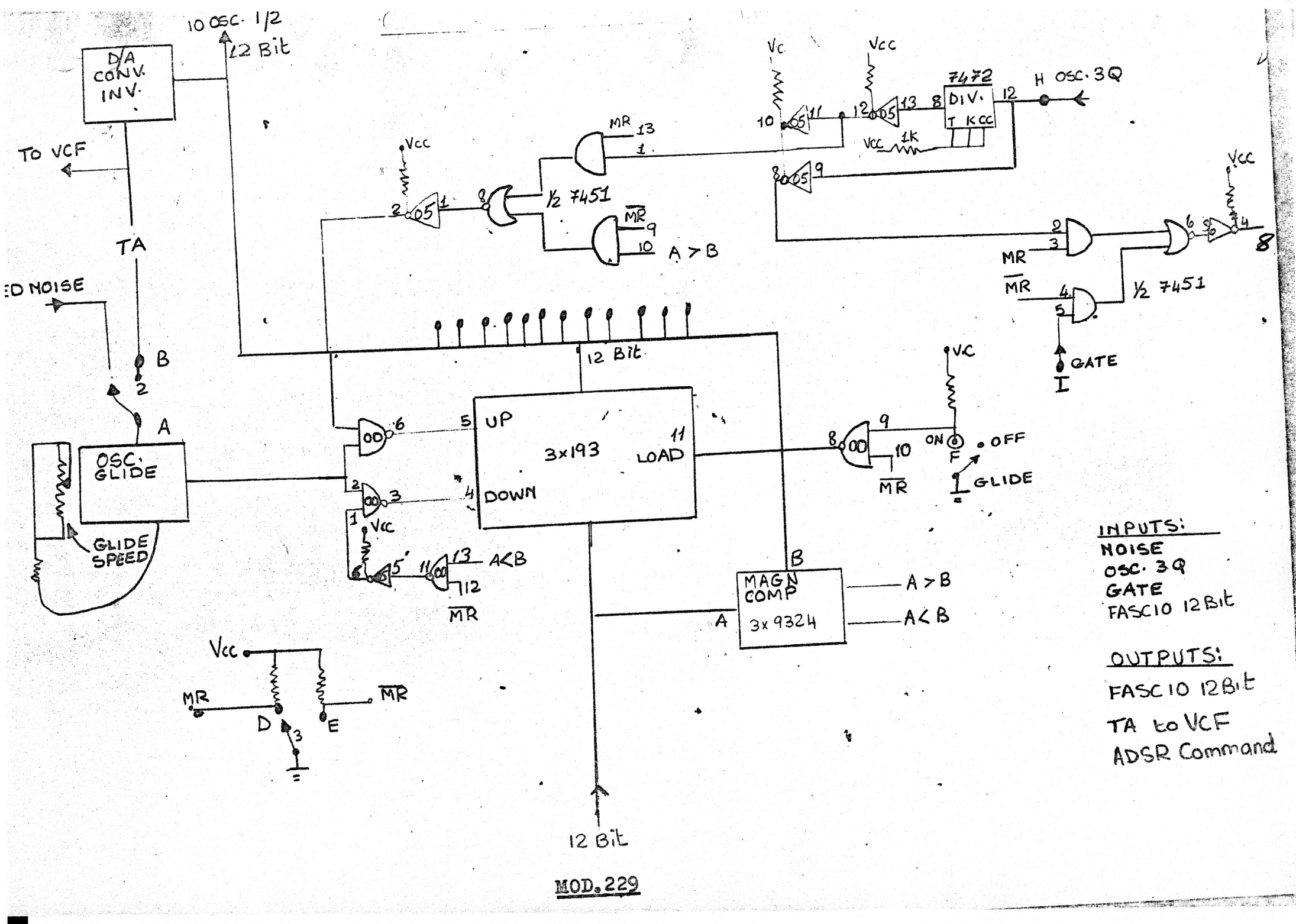
Level 0, which has been put, as can be seen from the diagram, in all of Pins 11 of 74193 and therefore, the code which is in input can be got at output, from where it is then sent to Osc. 1 and Osc. 2 and to a convertor. Digital in Analogic, (from one code a tension is extracted) which in its turn sends such tension to the oscillator of the GLIDE and to the VCF.

The convertor D/A has a generator at constant current which can be regulated at the trimmer, and a group of 12 resistors and 12 transistors commanded by GATE AND 7408 which draws out the output code of 74193.

Therefore it can be deduced that depending on the number of levels, 1 changes the value of R which comes through the constant current and therefore , at their heads, the value of 8V = DO highest (1° octave); 4V DO 2° Octave; 2V DO 3° Octave, 1V DO 4° Octave.
This tension depends on levels 1 because only the levels 1 can saturate the transistors and therefore, put more resistors in parallel between them. The CLOCK which has been formed by the GLIDE oscillator is present on Pin 4 and 2 of 7400 which can be sorted out of the two sections of 7400 in UP or DOWN.

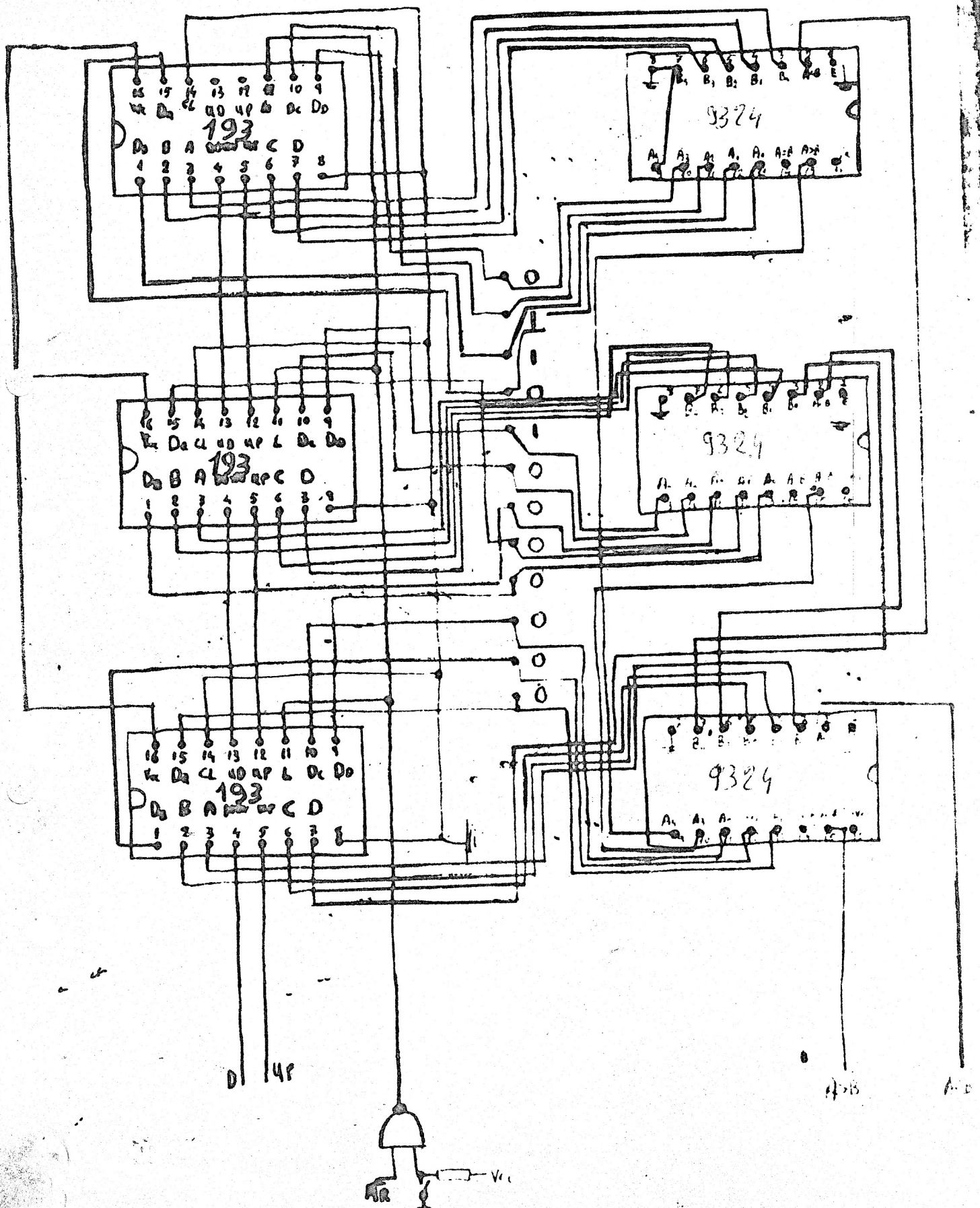
GLIDE

By inserting the GLIDE you have GLIDE ON at level 0 (Pin 9-7400) therefore the output 8 of 7400 goes to level 1, consequently also the Pin 11 of 74193 goes to 1 and therefore starts to count:
example: Let us suppose that the Code B has a hypthetic value 8 and that you send in A a code with a hypothetic value 6; at this point you can clearly see that B > A and that the counters which bring the CODE to output equal to that of input must count backwards.


10 OSC. 1/2
12 Bit
D/A CONV. INV.
TO VCF
TA
ED NOISE
B
2
A
OSC. GLIDE
GLIDE SPEED
12 Bit
UP
3x193
DOWN
LOAD
11
Vcc
MR
13
1
½ 7451
A > B
MR
9
10
A<B
12
MR
Vcc
MR
D
3
E
MR
12 Bit
Vc
Vcc
7472
DIV.
T K CC
H OSC. 3Q
1K
½ 7451
GATE
I
VC
ON
OFF
F
GLIDE
MR
MAGN COMP
3x9324
A
B
A > B
A<B
INPUTS:
NOISE
OSC. 3Q
GATE
FASCIO 12Bit
OUTPUTS:
FASCIO 12Bit
TA to VCF
ADSR Command

MOD. 229

PART OF MOD. 229



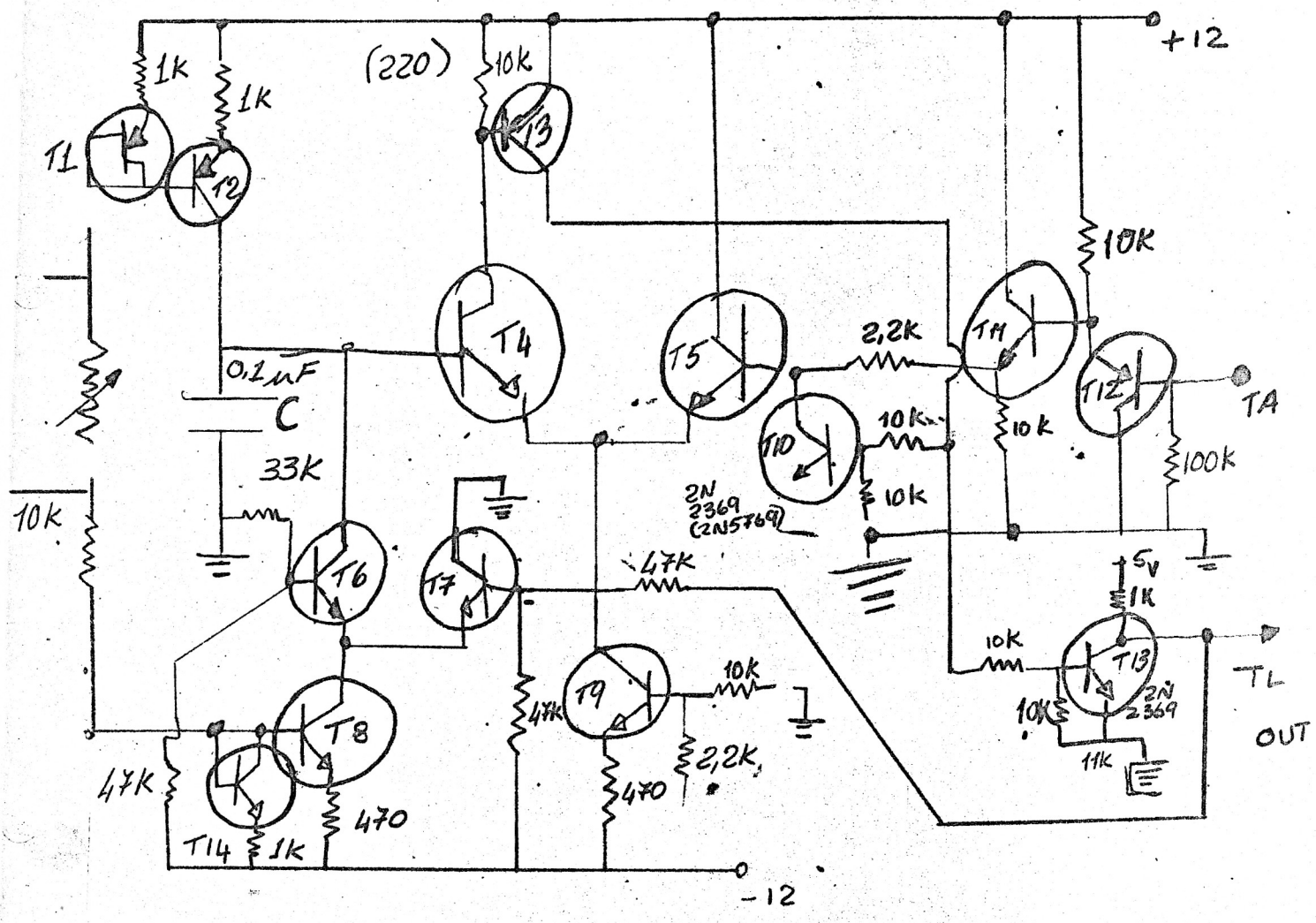
Now following the diagram, let us see if it is true that the counters really do count backwards. Having B>A the outputs of the comparators will be Pin 15, A>B = 0 and Pin 2, A<B = 1. The zero of Pin 15 of 9324 or 7485 is sent to Pin 10 of ½ 7451 and at the output of that GATE you will have 0 as also happens in the other gate because its Pin 13 = 0. Therefore the inputs of NOR are two zero's and its output Pin 8 is at level 1, therefore you have level 0 in Pin 2 of the inverter, and consequently also in Pin 5 of 7400.
At this point it seems clear how the output Pin 6 of 7400 and therefore also the Pin 5 of 74193 are blocked at 1, therefore the counters do not count forwards.
The Pin 2 of 7485 or 9324 which is at level 1, is sent to Pin 13 of 7400, which having the Pin 12 at level 1 will have at its output Pin 11 a level 0, which inverted becomes 1 in Pin 6 of the inverter and consequently is at level 1 also the Pin 1 of 7400. Therefore, in its output Pin 3, you have the CLOCK which is present in Pin 2 and which goes to Pin 4; two counters which count backwards.
In the instant that Code B from 8 goes down to 6 equalizing itself with that of A, also the output of the comparators A<B go to zero, therefore, you have a level 1 in Pin 11 of 7400, therefore zero in Pin 1 of 7400 which blocks the CLOCK and the counter stops counting.

If the Code in A had a value of 10 it is clear that the counters, to bring B equal to A, would have to count upwards until A = B, the instant in which the counters would block.
The time employed by the counters to bring A = B depends upon the speed of the CLOCK WHICH CAN be regulated by the speed potentiometer of the GLIDE.

The level 1 which you have in T with M Mod. 216 (on depressing one key), is brought into Mod. 229 Pin 5 of ½ 7451, which, when in normal condition has the Pin 4 at level 1 and the Pin 3 at level 0, therefore, the signal in Pin 4 passes and that which is present in Pin 2 becomes blocked. The level 1 in Pin 4 comes out the same as level 0 in Pin 6 of ½ 7457 and therefore you have Level 1 in Pin 4 of the inverter 7405.

GLIDE OSCILLATOR

MOD. 229



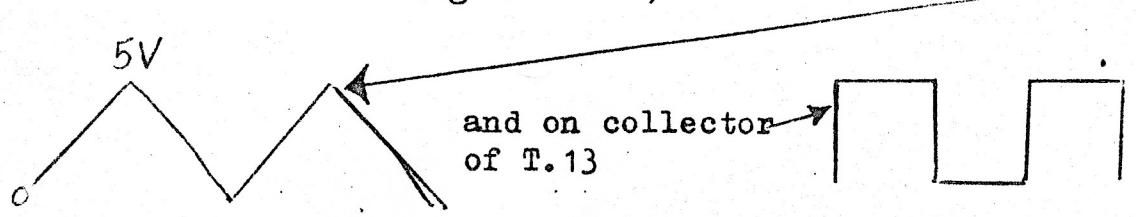
MUSIC RANDOM

With the M.R. switch inserted you have the following change over $\overline{MR} = 0$ MR = 1 the speed potentiometer GLIDE short circuits and in the place of the analogic tension, a RED NOISE signal is sent to the GLIDE oscillator.
From the diagram you will be able to understand that with MR = 0 and MR = 1, the counters, count only upwards and for half a period, because at Pin 1 of 7451 ½ the following wavelength arrives ⌐¬⌊ (which is obtained from Osc. 3 divided by 2 of 7472).

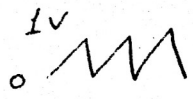
The command for the ADSR comes automatically from Pin 8 of 7405 to go out at Pin 4 of 7405. The keyboard in Music Random does not command the A.D.S.R anymore.

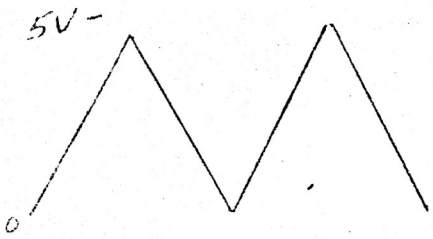
GLIDE OSCILLATOR

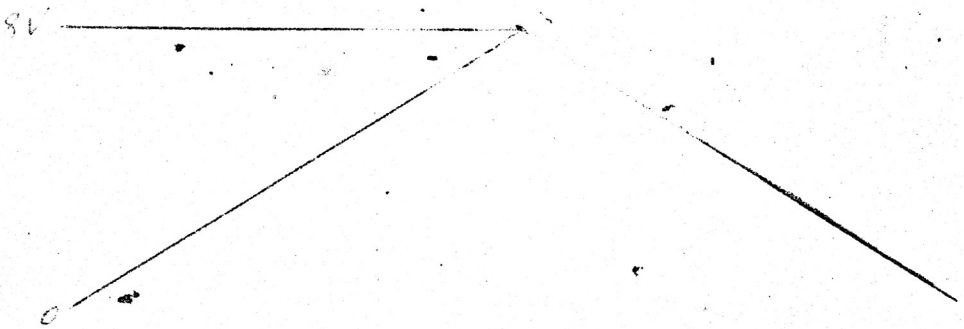
This is an oscillator which is based on the charge and the discharge of a capacitor at constant current which can be regulated by the speed potentiometer GLIDE and as a reference for the level which must be reached, you must use the tension coming from D/A CONVERTER. At the instant of turning on, the GLIDE starts charging up through the T.2 driven by the T.1 and arrives at up to 5 V., if the T.A of comparation is 5 V. This happens, because, if at the base of T.12 you put 5 V then at the base of T11 you will have 5,5V and at the base of T.5 you will have 5V, this level conducts the T.5 on T.4 up to the instant in which the level of C does not arrive at 5V., a level which conducts the T.4 on T.5. By conducting the T.4 , the T3 is also conducted which sends +12V to T10 (which saturates and therefore brings the base of T5 to zero) and to TR 13 which brings its collector to zero, (at this point it must be said, that before the saturation of T.13, of the differential couple T.6-T.7, T.7 conducted) and this potential lowers the base potential of TR7, which blocks while passing to conduct the TR6.(at this point the C discharges through the T6 and T8 at constant current/ The current which circulates in T6 and T8 is double in that which circulates in T2, because in those go the current T7 and that of C). When the C arrives at 0,10 - 0,2V the T5 conducts and blocks the T4, this blocks the T3, the T10 and the T.13 which however, makes the T7 conduct and blocks the T6 therefore, the C starts recharging again up to 5V and so on. Therefore the wavelengths are 2, at the heads of C



You have a clear result that the wavelength changes frequency and those at the heads of C also in width, to vary of TA to compare.







OSCILLATOR 1 AND OSCILLATOR 2

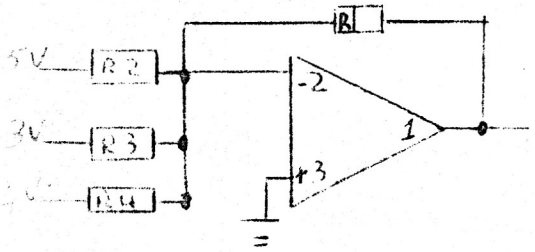
The oscillator of the Syntex is made up of:

3	74194 Programmed Counters UP/DOWN
3	74121 Monostables
1	7413
2	7400
3	OPERATIONALS MC 1458 or 72558

74194 are counters which with the Pin 5 at level 1 count downwards, these are called programmed, because as soon as they receive a level 0 in Pin 11 they start to count from

the number of Code present in the inputs. 15 - 1 - 10 - 9 Every time they arrive at 0 the Pin 13 gives a level 0. The Pin 14 is the input of CLOCK, the Pin 4 must be kept at level 0.

MC1458 are operational amplifiers which are used as amplifiers and adders of more signals, in this case the output is inverted and the input must be the negative one:

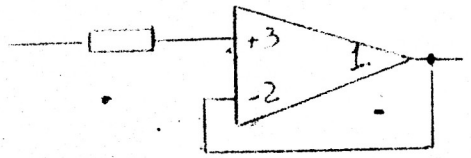


R1 = 10K; R2 = R3 = R4 = 5K

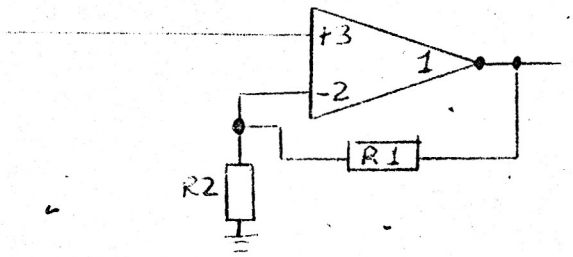
$G1 = \frac{R1}{R2} = 2$; $G2 = \frac{R1}{R3} = 2$; $G3 = \frac{R1}{R4} = 2$

The output of Pin 1 is the inverted sum design of three levels

- 10
- 6
+ 8
- 8 V

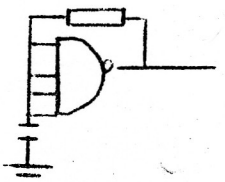


An emitter follower is connected in this way

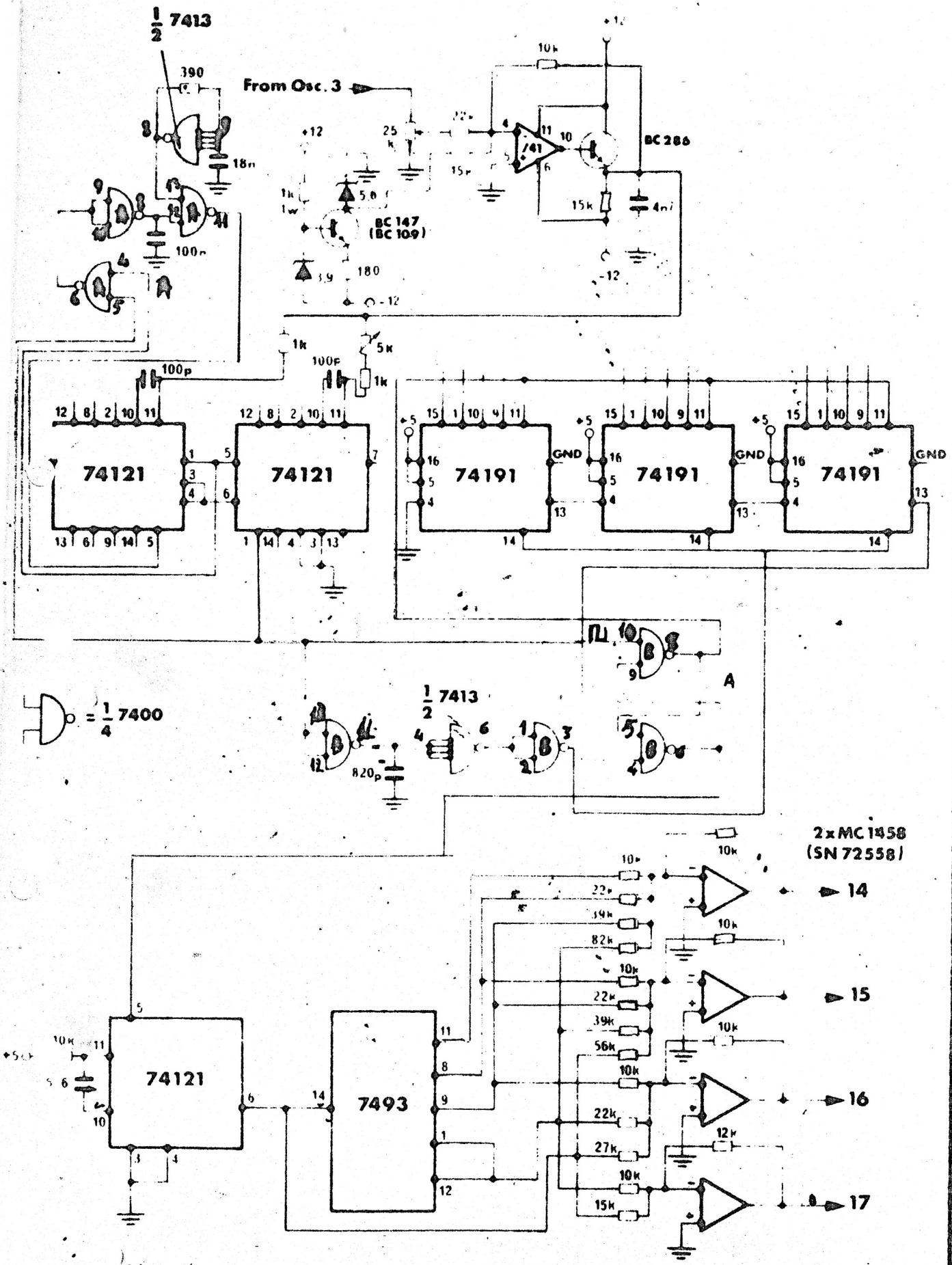


A simple amplifier is connected in this way with $G = \frac{R1}{R2}$

The oscillator oscillates for half of the two 74121 connected in reaction, in such a way as to form an Astable. To win the entry and to be certain that you will always have oscillation an auxillary oscillator has been used, formed with a section of 7413



WHICH oscillates at 270 KHz



OSCILLATOR 2 . Mod. 223

DWG - F

Mod. SYNTEX			SERIAL No		
WELSON	CODE	DRAWN By [illegible]	REVISION		
		CHECKED By S. Mansfield	DATE	31	7 74

Now let us suppose that in the instant of switching on, the Pin 1 of the two 74121 is brought contemporarily to level 1 (if there was no auxiliary oscillator the Astable of the two 121 would be blocked) which we find at Pin 4 and 5 of 7400 (A) therefore in its output Pin 6 you have level 0 which being present in Pin 9 and 10, allows a level 1 in Pin 8 and also therefore in Pin 12, which allows the oscillator present in Pin 13 to travel through the Pin 11 which is connected to Pin 5 (input of MON) this puts its Pin 1 to 0 overbalancing the system and therefore allows them to oscillate. As the signals of output of the two Pin 1 of the 74121 (when oscillating) are 180° dephased the Pin 6 of 7400(A) will always be 1 with the consequent level 0 at Pin 12 and therefore the Pin 11 fixed at level 1.

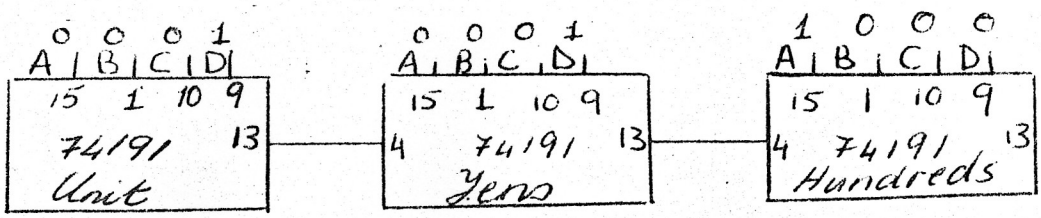
This indicates that when the oscillator of the 74121 oscillates, that of the auxiliary is blocked. In the instant of switching on, the Pin 13 of the last 74191 of the three placed in fall, gives an 0 which connected to Pin 4 of integrated circuit B allows a level 1 at Pin 6, which connected to Pin 9 makes an impulse go out at Pin 8, which connected to the Pins 11 of the 74191 brings all of the Pin 13 of the same to 1 (this in the negative half period) while as the positive half period arrives in Pin 8 and therefore in Pin 5 and being 1, the Pin 4 has 0 at Pin 6 and at Pin 9, this blocks the output of Pin 8 at level 1.

The CLOCK at the Pin 14 of the 74193 arrives with delay in respect to the 0 of the Pin 11, because it passes across a line of delay formed by section 13 - 12 and 11 of B from 7413 ½ and of section 1 - 2 and 3 of B.

As soon as 0 arrives at the Pin 11 of 74191 these prepare to start counting downwards starting from the Code present at that instant in the Bit of input of 74191.

Example: Code 392 = 256 +
128 +
8
392

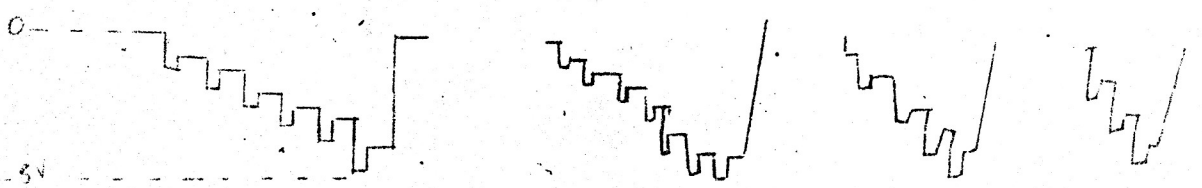
2048	1024	512	256	128	64	32	16	8	4	2	1
0	0	0	1	1	0	0	0	1	0	0	0
	Hundreds				Tens				units		



Those of the unit and of the tens start from 8 while those of the hundreds start from 1

a	8	0	15	0	15	0	15	0	15	0	15	0	15	0	15	0	15	0	15	0	15	0	15	0	15	0
D		8		7		6		5		4		3		2		1		0	15	14	1					0
C	-		-		-		-		-		-		-		-		-	1								0

When the three Pin 13 of the 74191 have 0 you have an 0 at Pin 4 of B and therefore 1 at Pin 6 always of B which goes to Pin 9 of B and to input Pin 5 of monostable 74121 the output of which drives a divider 7493 at 4 states.
On every 392 impulses you have one going towards the monostable, therefore dividing the frequency of the oscillators by 392 you obtain the audio frequency. The wavelengths coming from 7412 and 7493, initially come through half the resistors and are sent to 4 operationals, the wavelengths of which in output are the following:



The function which works this small group characterized by operational 741 and by two transistors is that of supplying the oscillators of the two 74121 with a continuous tension upon which the wavelength of oscillator 3 later becomes summed up to make the Vibrato.

VCF - VCA MOD.238

In this circuit board you can find the filter VCF and the preamplifier VCA.
The VCF is a filter commanded in tension which uses filter cells made from transistors and capacitors, the transistors are changeable resistors, changing with the current. The working control of a filter can be regulated by the two differentials T7 and T8, the base of T7 is that which receives the commands for regulation of the filter. When the potentiometer FR is at its lowest point it sends a negative tension to the base of T.7

Therefore only T8 can conduct and if no current is passing through T7, neither can it pass through the filter, therefore no signal can be passed out.

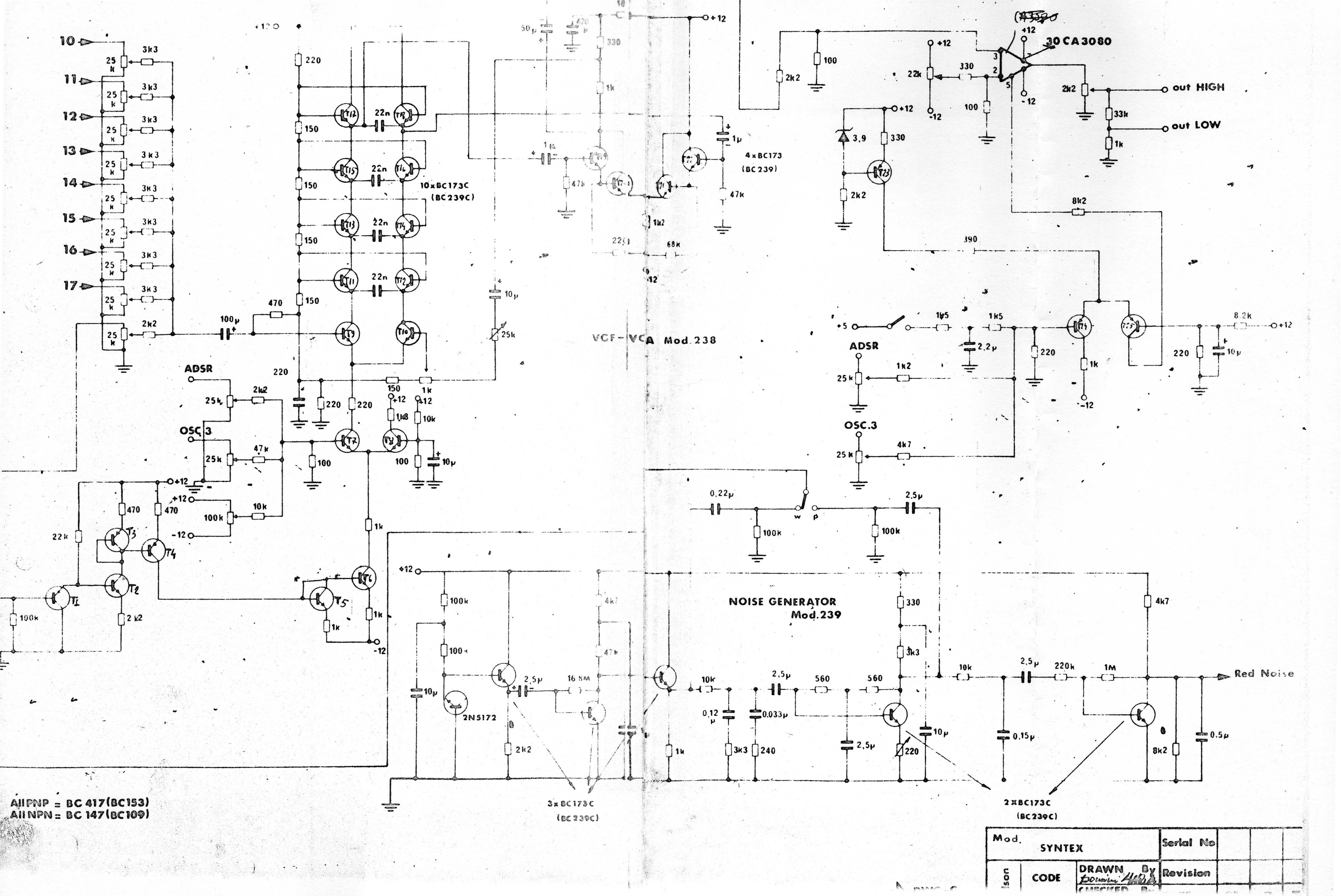
T8 has a fixed base of +120mV. By moving the FR potentiometer you can move the potential of the base of T7 and conduct gradually always more, so that upon arriving, only he is conducting and T8 becomes blocked.
In this condition the filter is fully open and very bitter sounds can be heard.
The commands to the filter are given by the FR POT. by the Amount Pot. ADSR and by the Amount Pot. OSC. 3.
The group made up from T1 - T2 - T3 - T4 - T5 - T6 are used for supplying constant current to the couple T7-T8. This current which is constant is not fixed, it can be said, that it changes depending on the key depressed, however, once you have reached a value, this always remains constant.
The current in the T7-T8 couple changes because an analogic tension arrives at the base of T1 generated by the D/A Converter of Mod. 229 which changes for every key. Some levels in the various transistors for one TA = 5 and with the FR potentiometer as high as possible Q + 12 V. Base T1 = 5V Base T2 = 5,5 Collector T2 = 9,5V Collector T4 = - 10V. Collector T6 = - 3V Emitter Coppia T7 - T8 = - 0,5V at heads of 220Ω of collector of T7 = +200 mV

POLARIZATION OF TRANSISTORS IN FILTER

Bases T9 and T10 = 2V Bases T11 - T12 = 4V Bases T13-T14 =5,5V
Bases T15 - T16 = 7V Bases T17 - T18 = 9 V

The signal which comes out through the filter crossing two capacitors goes into a differential couple T19-T20 and T21-T22, in the collector of T19-T20 there must be about 6V for a good gain, this tension can be regulated acting on the resistor of 68K put between the base of T21 and the emitter of T22, by increasing it the tension in collector T19-T20 is increased, by decreasing, the tension is decreased.

The filter is a low pass, which can become an adjustable Q Notch Filter more or less selective depending upon the position of the Q potentiometer. It can become so selective that on regulating the Trimmer from 1K it oscillates.



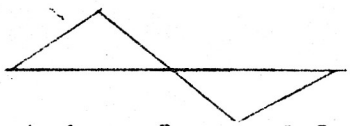
VCF-VCA Mod. 238
10×BC173C
(BC239C)
4×BC173
(BC 239)
30 CA3080
out HIGH
out LOW
ADSR
OSC.3
NOISE GENERATOR
Mod. 239
Red Noise
2N5172
3×BC173C
(BC239C)
2×BC173C
(BC239C)
All PNP = BC 417 (BC153)
All NPN = BC 147 (BC109)
Mod. SYNTEX
Serial No
CODE
DRAWN By
CHECKED By
Revision

The VCA is an amplifier which is controlled in voltage, the integrated circuit is the CA3080. To drive the VCA, a generator of constant current T28 is used and also a differential couple T24 and T25, so that the voltage in it may be proportioned. The base of T25 is fixed at + 200mV, while the base of T24 has a tension which can be regulated externally: through the Pot. Amount ADSR; the Pot Amount Osc.3 (modulation of largeness - tremolo) and the Initial Volume pushbutton. Some notes of measurement with the Initial volume inserted:-

at heads of R = 390 put on emitters of the T24-T25 V = 4V
" " " R = 8kz " " " " " T25 V = 12V

ADSR OSC. 3 MOD. 282

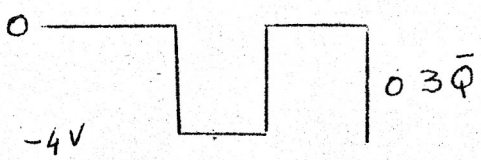
The oscillator 3 and the modulation oscillator and its working are exactly the same as the GLIDE oscillator, the only difference being that the compared tension is fixed at +5V.
Also, this oscillator has a speed potentiometer and generates two wavelengths: triangle and square.
The output of the triangular wavelength goes into a section of the 1° operational MC 1458 used as an emitter follower and then into the second section, the input of which is inverted, a negative tension is also included so that the triangular wavelength in output will be half over zero and half under zero:

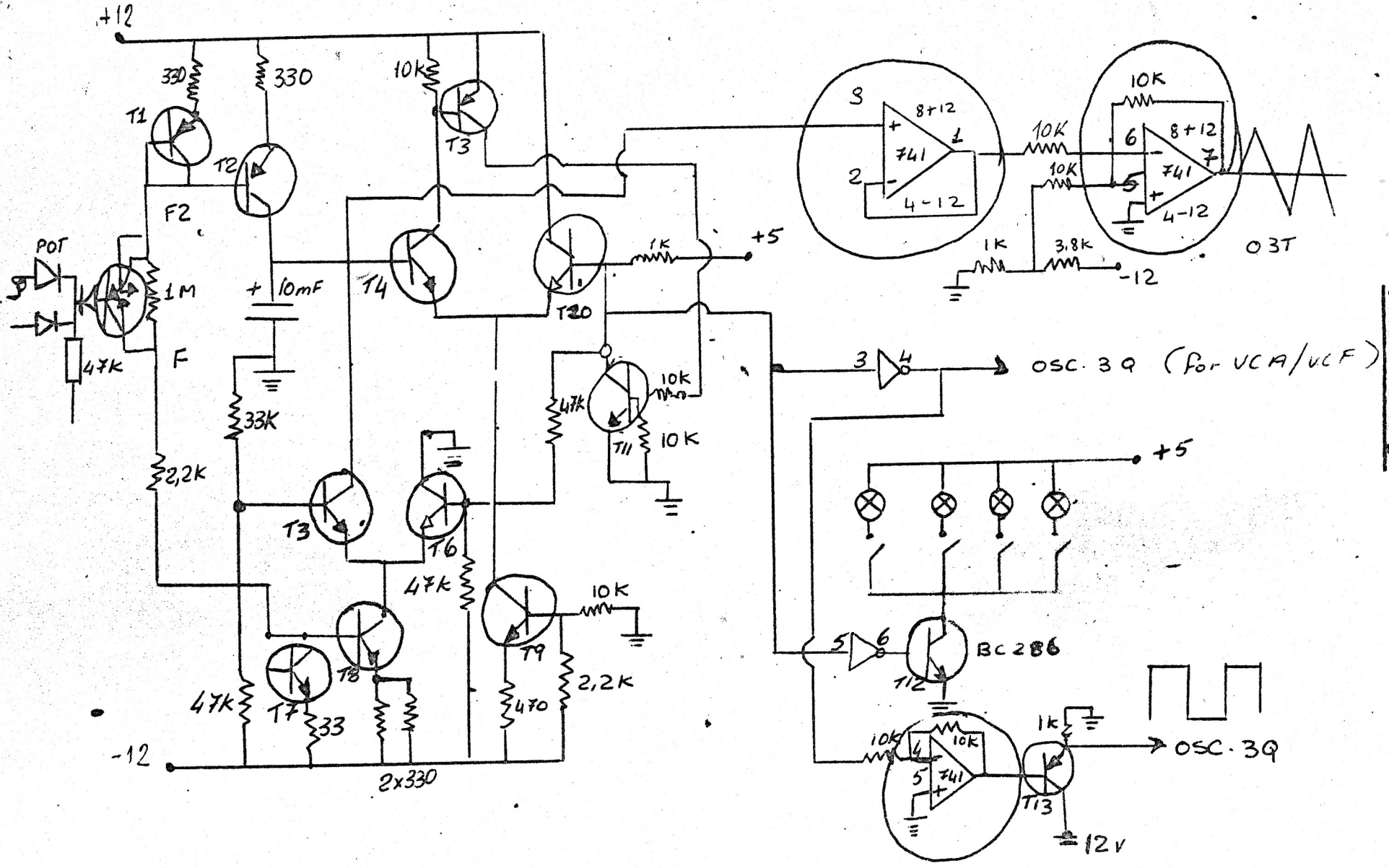


this output is used for triangular modulation and is sent to Osc. 1, Osc. 2 , VCF and VCA, and it is named 03T.

The square wavelength passes through an inverter and , the output which is named 03Q is used for the modulation and square wave for the VCA and VCF.
The square wave output also goes into another inverter which in its turn drives the TR BC286, which is used for lighting the lamp when the modulation has been inserted at the switch.

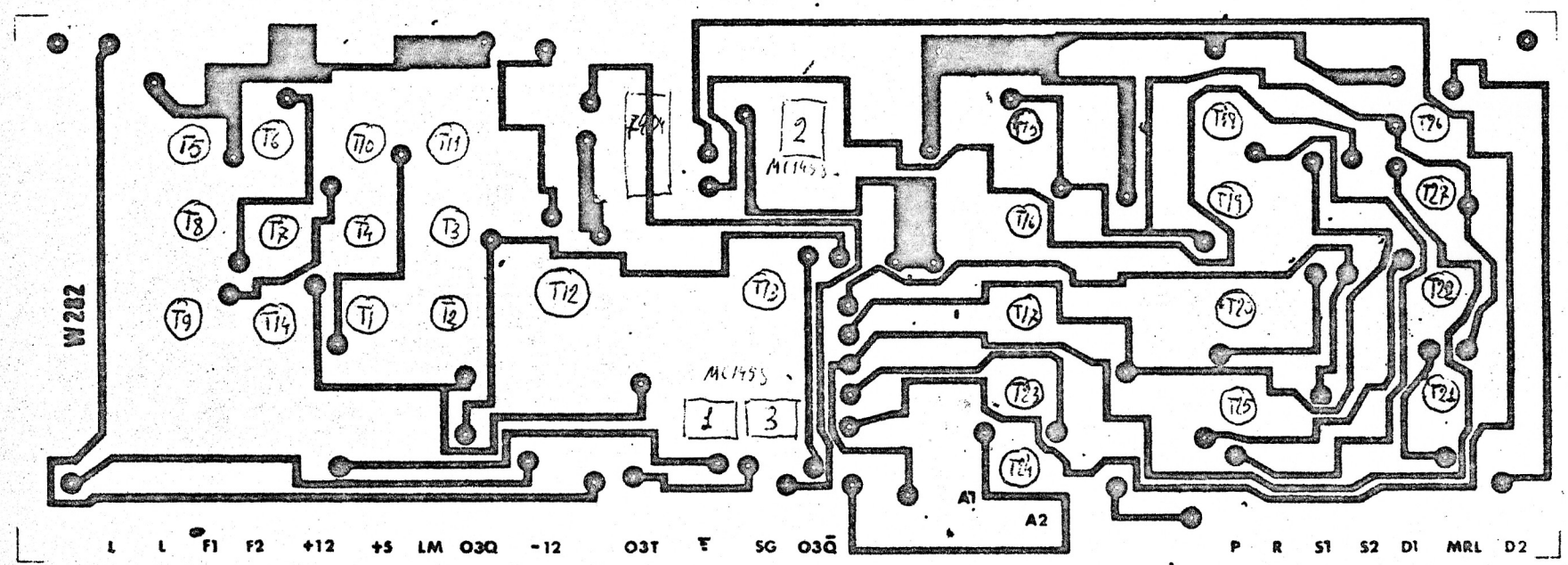
The output 03Q besides going to VCF and VCA, also goes to an inverted input of operational 72741, the output of which drives an emitter follower, from this emitter, negative square wavelengths com out which are named 03$\bar{Q}$ and these are used for modulating Osc. 1 and Osc. 2





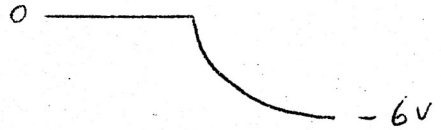
OSCILLATOR 3

MOD. 282


W282
T5
T6
T10
T11
T8
T7
T4
T3
T9
T14
T1
T2
T12
T13
2
MC1455
1
3
T18
T19
T16
T17
T20
T21
T22
T23
T24
T25
A1
A2
L L F1 F2 +12 +5 LM O3Q -12 O3T E SG O3Q̄ P R S1 S2 D1 MRL D2

ENVELOPE GENERATOR ADSR

On depressing a key, the impulse generated from T with M is passed to the circuit board Mod. 229, and from this it is then transferred to Pin 1 of 7404 of Mod. 282, which provides an 0 to Pin 2. Therefore, the T15 conducts and its collector is brought to +5V, a level which enables the T16 to conduct, This T16 brings its collector to the same potential of the emitter, which is -6V, at this point the capacitor CATT is arged through the potentiometer of ATT the 47 ∿ and the T16 at -16V.



T17 is an emitter follpwer, therefore, in its emitter at the base of T18 you have -5,5V, therefore, the T18 which has the emitter at -4,2V conducts and brings a more positive level to the base of T19 and consequently this conducts. By conducting T19, this also conducts T20 which brings its collector to level +12V. This tension is then divided between the 560 and the Sustain potentiometer, the level of the division is then sent to the base of T21 therefore, in its emitter it has the same tension of the base minus the Vbe, and it is at this level of tension that the C Decay is set, a level which is lowered to a Vbe of T22 and increased to a Vbe of T27, at which point, through an R = 1 M it goes and mixes with the level of C attack on the inverted input of an operational, which inverts the two signals and does the sum. Let us suppose that the level of stationing between the 560 ∿ OF T20 and the Sustain pot. is 4V, the level at the heads of = 220K of T27 will be 3,5 with charge exponential

FIG. B now this

wavelength through an R = 1 is sent to the inverted input of the operational as the wavelength of the attack, therefore at the output of the operational we shall have the following wavelength:

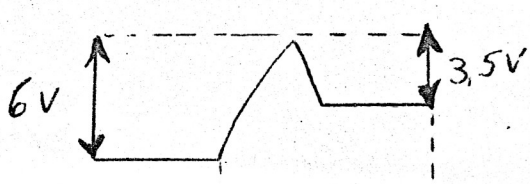
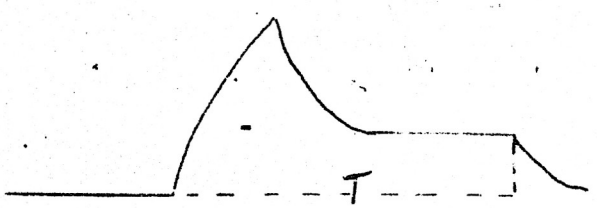


FIG. C

This wavelength passes from an emitter follower to its emitter, the C Release Pot. is connected, and through an 4K7 the T25 which upon depressing a key, receives a level 1 in its base and therefore, is saturated for the period of time of the formation of wave of Fig. C in such a way as to form together with CR a group RC with very small constant (quick) in such a way as to follow point point Fig. C with deforming it.
On releasing the key, the T25 opens, and the period of time for discharge of CR is commanded by the Release Pot. this time very small in respect to T25 in opening.
As the T25 opens, the T23 closes, so that, part of the circuit of T24 is excluded from the process of discharging of CR.
The T26 is commanded in the same way as T25. Its function is to drive M.R lamps when its switch is inserted.
The wavelength at the heads of CR enters the operational input 3, not inverted, and therefore, on output we have the same wavelength increased in gain of operational.



			F E D C B A	2048 1024 512 256 128 64 32 16 8 4 2 1	
TOP C	DO	3	0 0 0 0 1 1	0 0 0 1 1 0 0 0 0 1 1 1	391
	SI	4	0 0 0 1 0 0	0 0 0 1 1 0 0 1 1 1 1 0	414
	LA#	5	0 0 0 1 0 1	0 0 0 1 1 0 1 1 0 1 1 1	439
	LA	6	0 0 0 1 1 0	0 0 0 1 1 1 0 1 0 0 0 1	465
	SOL#	7	0 0 0 1 1 1	0 0 0 1 1 1 1 0 1 1 0 1	493
	SOL	8	0 0 1 0 0 0	0 0 1 0 0 0 0 0 1 0 1 0	522
	FA#	9	0 0 1 0 0 1	0 0 1 0 0 0 1 0 1 0 0 1	553
	FA	10	0 0 1 0 1 0	0 0 1 0 0 1 0 0 1 0 1 0	586
	MI	11	0 0 1 0 1 1	0 0 1 0 0 1 1 0 1 1 0 1	621
	RE#	12	0 0 1 1 0 0	0 0 1 0 1 0 0 1 0 0 1 0	658
	RE	13	0 0 1 1 0 1	0 0 1 0 1 0 1 1 1 0 0 1	697
	DO#	14	0 0 1 1 1 0	0 0 1 0 1 1 1 0 0 0 1 1	739
HI C	DO	19	0 1 0 0 1 1	0 0 1 1 0 0 0 0 1 1 1 1	783
	SI	20	0 1 0 1 0 0	0 0 1 1 0 0 1 1 1 1 0 1	829
	LA#	21	0 1 0 1 0 1	0 0 1 1 0 1 1 0 1 1 1 1	879
	LA	22	0 1 0 1 1 0	0 0 1 1 1 0 1 0 0 0 1 1	931
	SOL#	23	0 1 0 1 1 1	0 0 1 1 1 1 0 1 1 0 1 1	987
	SOL	24	0 1 1 0 0 0	0 1 0 0 0 0 0 1 0 1 0 1	1045
	FA#	25	0 1 1 0 0 1	0 1 0 0 0 1 0 1 0 0 1 1	1107
	FA	26	0 1 1 0 1 0	0 1 0 0 1 0 0 1 0 1 0 1	1173
	MI	27	0 1 1 0 1 1	0 1 0 0 1 1 0 1 1 0 1 1	1243
	RE#	28	0 1 1 1 0 0	0 1 0 1 0 0 1 0 0 1 0 1	1317
	RE	29	0 1 1 1 0 1	0 1 0 1 0 1 1 1 0 0 1 1	1395
	DO#	30	0 1 1 1 1 0	0 1 0 1 1 1 0 0 0 1 1 1	1479
MY DC	DO	35	1 0 0 0 1 1	0 1 1 0 0 0 0 1 1 1 1 1	1567
	SI	36	1 0 0 1 0 0	0 1 1 0 0 1 1 1 1 0 1 1	1659
	LA#	37	1 0 0 1 0 1	0 1 1 0 1 1 0 1 1 1 1 1	1759
	LA	38	1 0 0 1 1 0	0 1 1 1 0 1 0 0 0 1 1 1	1863
	SOL#	39	1 0 0 1 1 1	0 1 1 1 1 0 1 1 0 1 1 1	1975
	SOL	40	1 0 1 0 0 0	1 0 0 0 0 0 1 0 1 0 1 1	2091
	FA#	41	1 0 1 0 0 1	1 0 0 0 1 0 1 0 0 1 1 1	2215
	FA	42	1 0 1 0 1 0	1 0 0 1 0 0 1 0 1 0 1 1	2347
	MI	43	1 0 1 0 1 1	1 0 0 1 1 0 1 1 0 1 1 1	2487
	RE#	44	1 0 1 1 0 0	1 0 1 0 0 1 0 0 1 0 1 1	2635
	RE	45	1 0 1 1 0 1	1 0 1 0 1 1 1 0 0 1 1 1	2791
	DO#	46	1 0 1 1 1 0	1 0 1 1 1 0 0 0 1 1 1 1	2959
LOW C	DO	47	1 0 1 1 1 1	1 1 0 0 0 0 1 1 1 1 1 1	3135

KEYBOARD ENCODER & MEMORY Mod. 216

DATA INPUTS (8)

+5V.

8 CHANNEL 74151 MULTIPLEXER

DATA SELECT (3)

MULTIPLEX O/P's 1-6, 11, 12.

7430 8 INPUT NAND.

4n7

TRIPLE 3 I/P

1/3 7410 NAND.

390

10n

1/2 7413 DUAL SCHMITT TRIGGER

680pF

1K

470

700 KHZ

1/3 7410

MONO-STABLE 74121 MULTIVIBRATOR

2µ2

33K

B INPUT

Q

3K3

470n

1/2 7413 GATE

Key Down

Key up

1/6 7405 HEX INVERTER (open collector)

29722 SNB746F

100KHZ

50KHZ

25KHZ

4KHZ

3KHZ

12.5KHZ

2K2

3K3

470pF

1/3 7410

UP/DOWN 4 BIT BINARY COUNTER 74193 LOAD CARRY BORROW

74193

DUAL 1 LINE - 4 LINE DE-MULTIPLEXER 74155

CHIP ENABLE LINES

Key Down

Key up

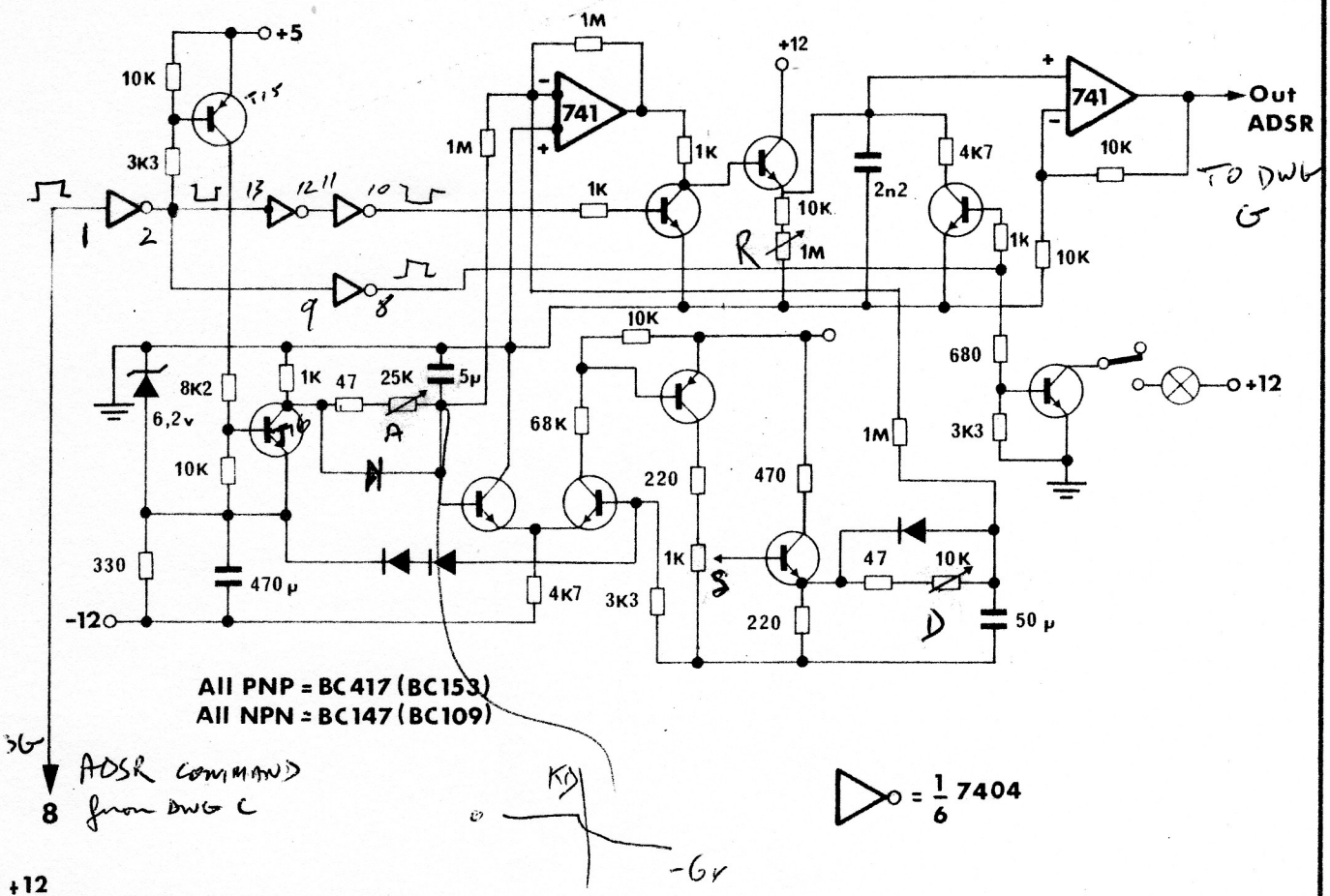
1 2 3 4 5 6 7

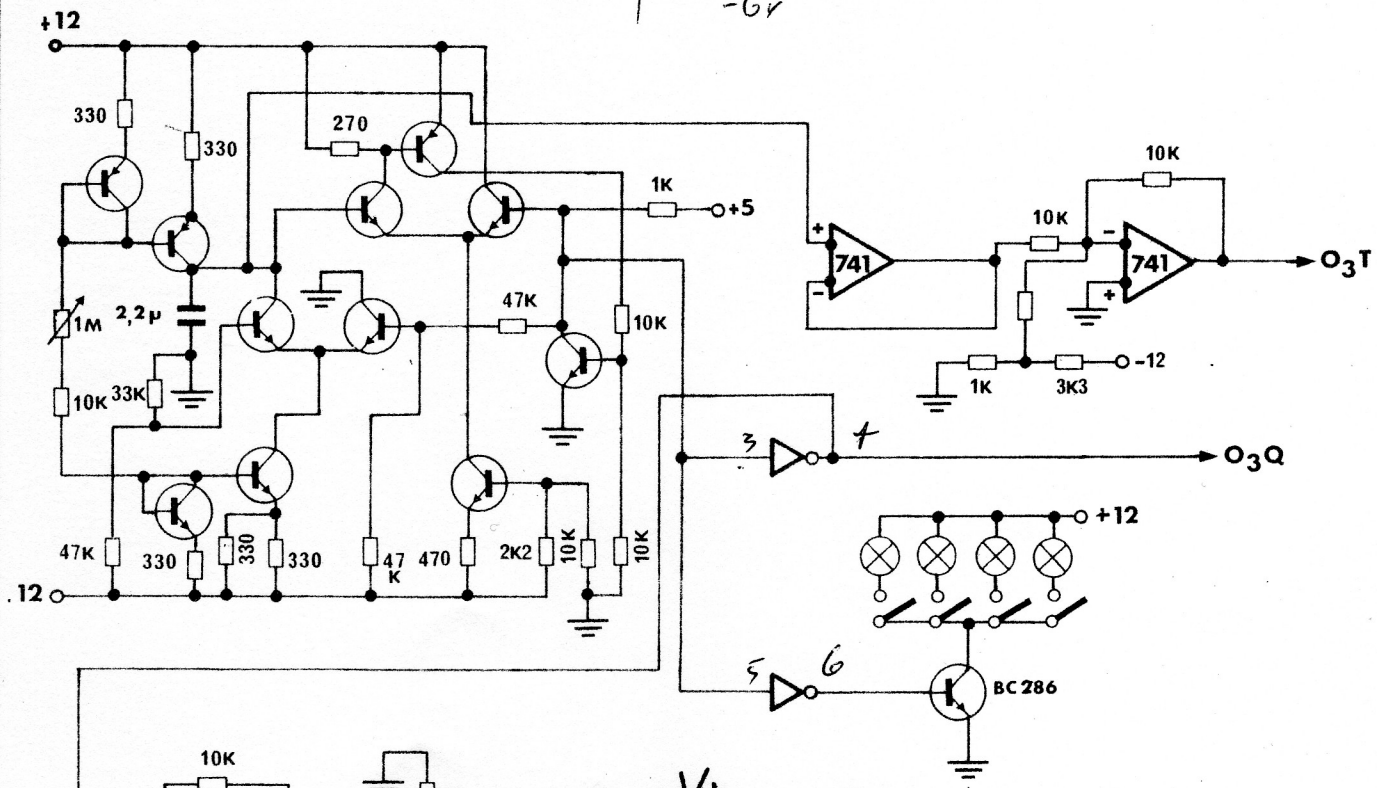
CPDT S/W

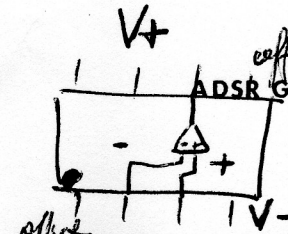
HOWC	111101	HOW G	000101
MIDC	110001	MID G	000110
TOPC	110010	TOP G	000100
HIGHC	111000		

DWG-A

Mod. SYNTEX			SERIAL No
SON	CODE	DRAWN By	REVISION







ADSR GENERATOR & OSCILLATOR 3
Mod.234

Mod. SYNTEX			SERIAL No		
DWG - B	CODE	DRAWN BY	REVISION		
		CHECKED BY	DATE	31	7	74

CODE CONVERTER 1 MASKED

CODE CONVERTER 2 MASKED

A.D.S.R COMMAND TO DWG B

Key Down

1/2 7451

DUAL 2-WIDE 2-I/P AND-OR INVERT GATE

from DWG 1 (O/P of Glide Osc)

D/K MASTER-SLAVE CLOCK 7472 FLIP-FLOP

GLIDE ON OFF

MEMORY

74193 UP/DOWN BINARY COUNTER 4 BIT.

LOAD when in Static

CLEAR

CLOCK UP

CLOCK DOWN

5 BIT COMPARATOR 9324

Inhibit Clocking

2 1 5
0 0 A=B
1 0 COUNT DOWN
0 1 COUNT UP

2048 1024 512 256 128 64 32 16 8 4 2 1

3x7408

470 1k 2k 4k 8k 16k 32k 64k 128k 256k 512k 1024k 2048k

Q x12 = BC173C (I.T.T)

741

-12 1k 560 1k DZ 3,9v 1k2 2k2 2x BC417 (BC153) BC147 (BC109)

To VCF DWG G

= 1/6 7405

= 1/4 7400

CODE CONVERTER & CONTROL CIRCUIT

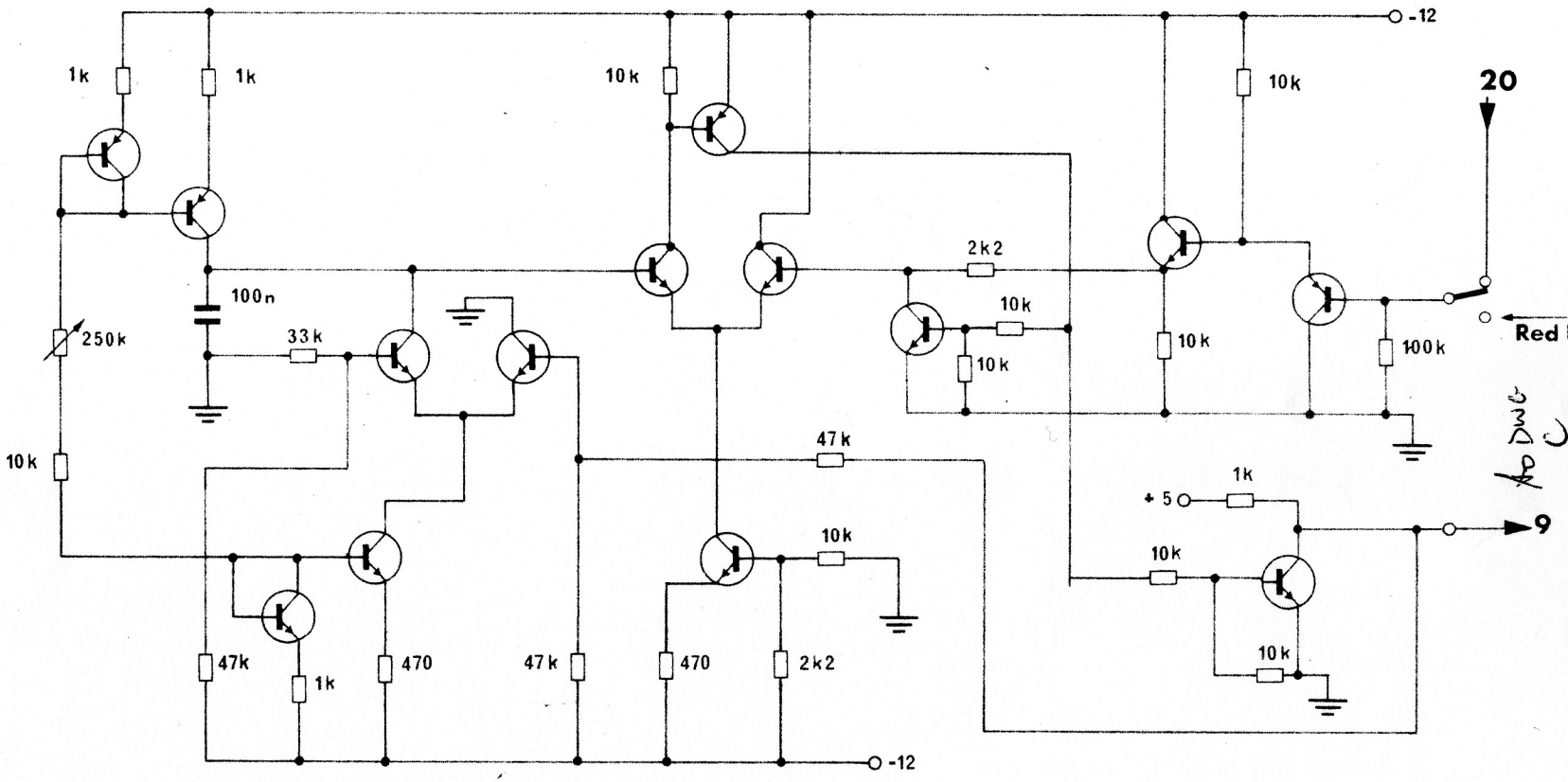
Mod.229

+ blue osc

Mod. SYNTEX		SERIAL No			
	DRAWN By	REVISION			

PORTAMENTO (GLIDE) OSCILLATOR

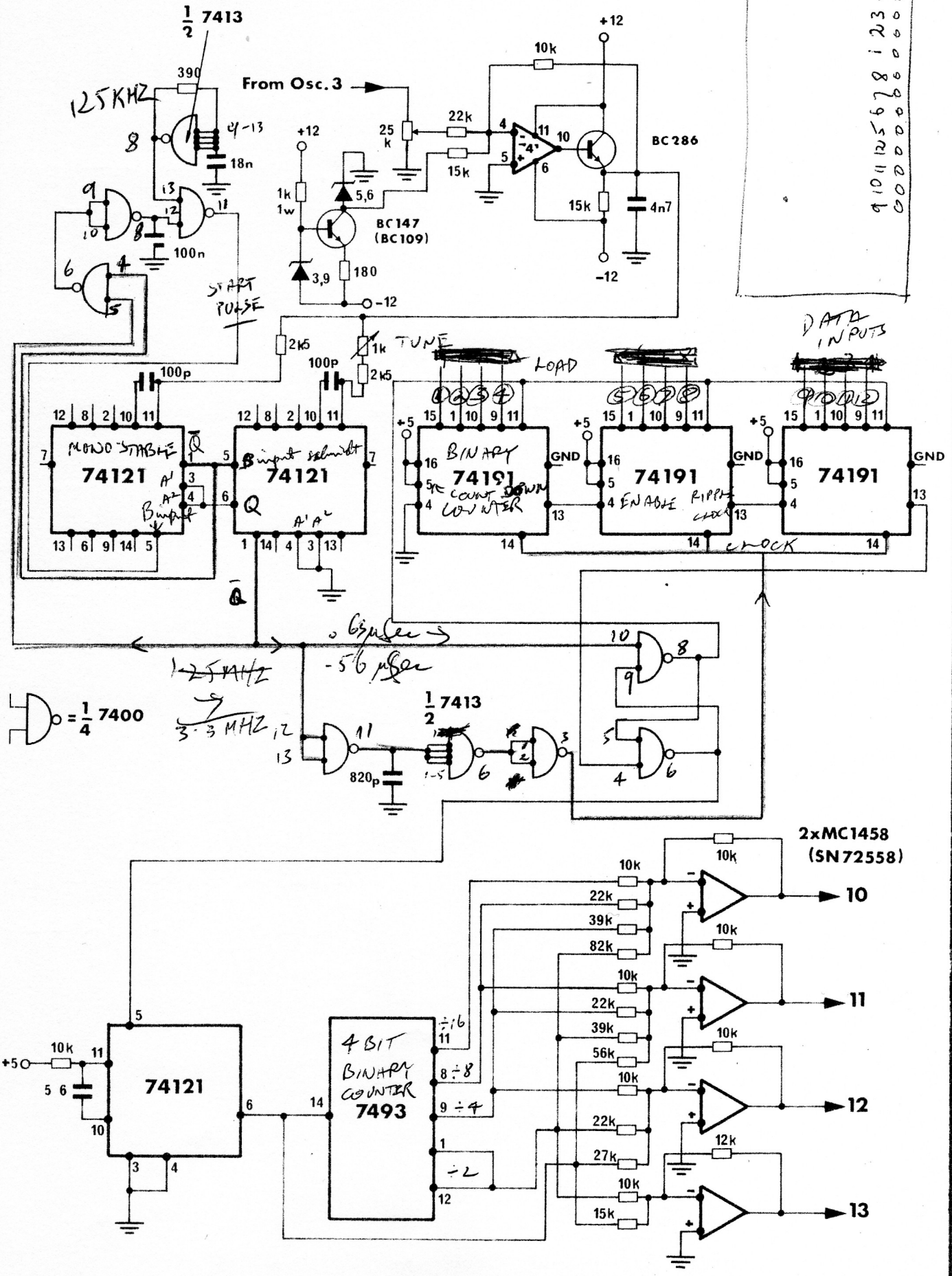
Mod.229 (on control P.C.B.)



All PNP = BC417 (BC153)
All NPN = BC147 (BC109)

		74
		7
		31
SERIAL No	REVISION	DATE
Mod SYNTEX	DRAWN By	CHECKED By
	CODE	
	WELSON	

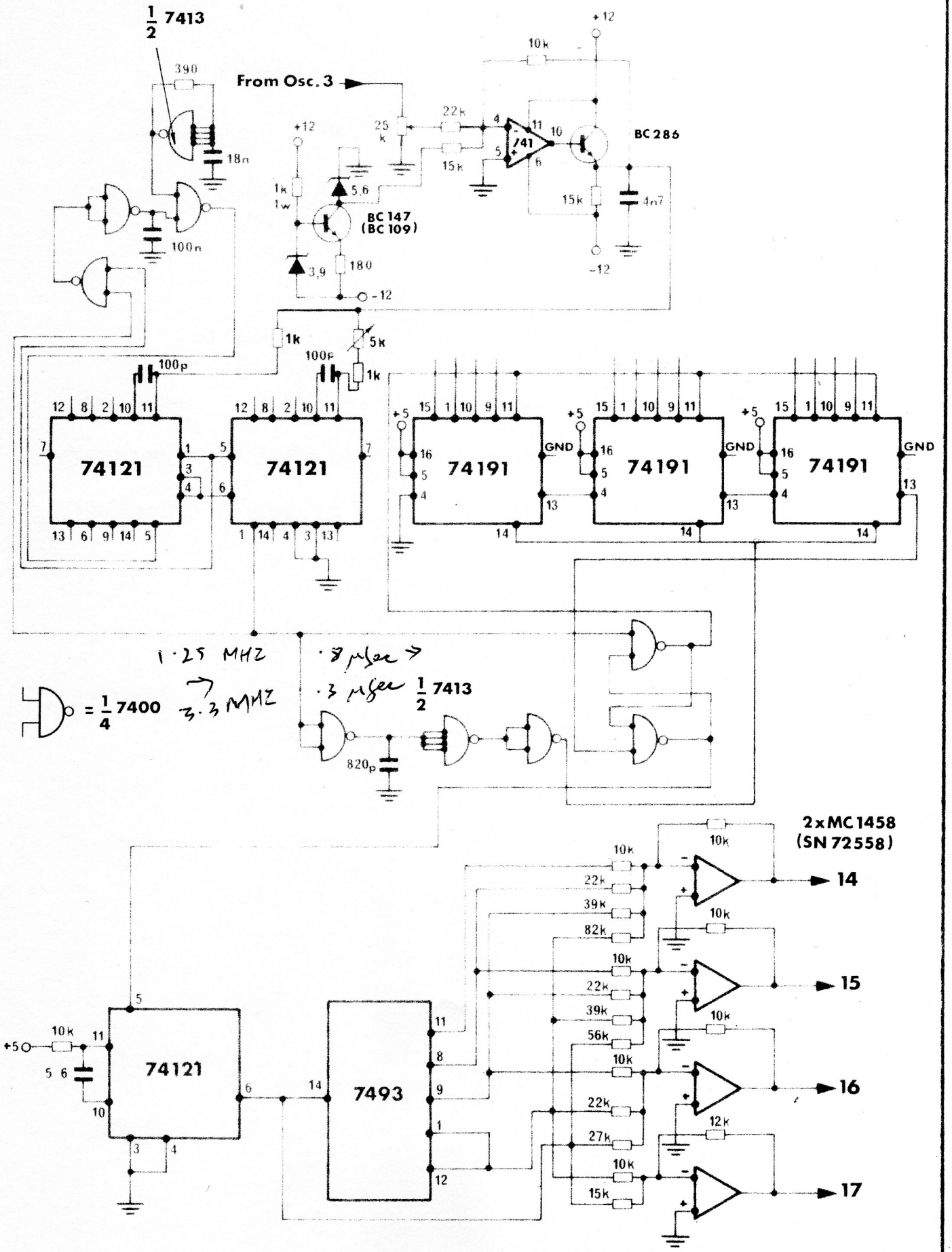
DWG-D



OSCILLATOR 1 Mod.223

Mod. SYNTEX			SERIAL No			
WELSON	CODE	DRAWN By	REVISION			
		CHECKED By S. Mendinelli	DATE	31	7	74

DWG-E



OSCILLATOR 2 Mod.223

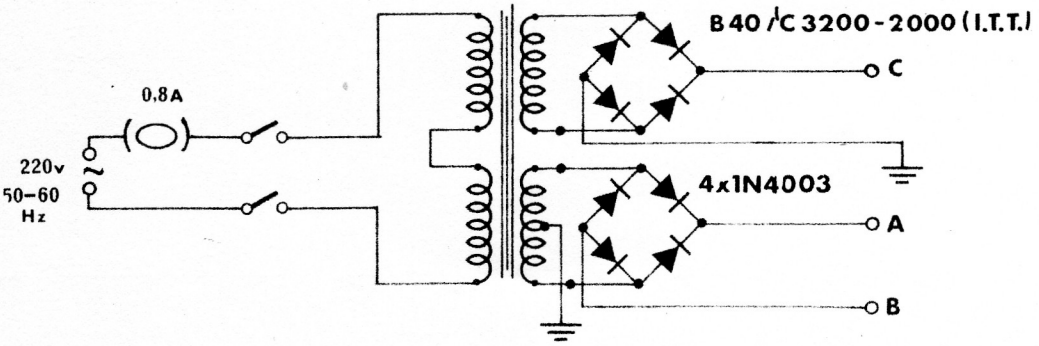
DWG - F

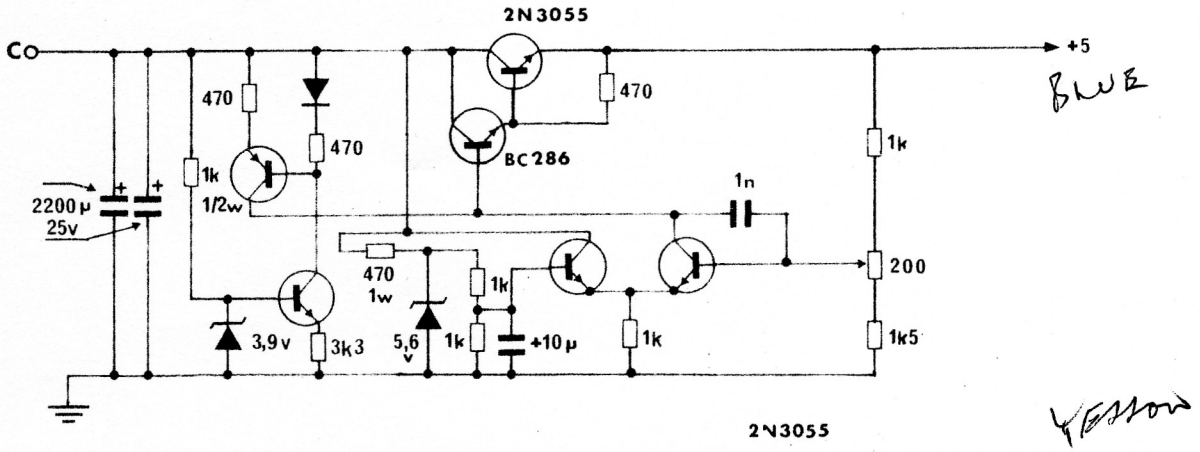
Mod. SYNTEX			SERIAL No		
VELSON	CODE	DRAWN By [illegible]	REVISION		
		CHECKED By [illegible]	DATE	31	7	74

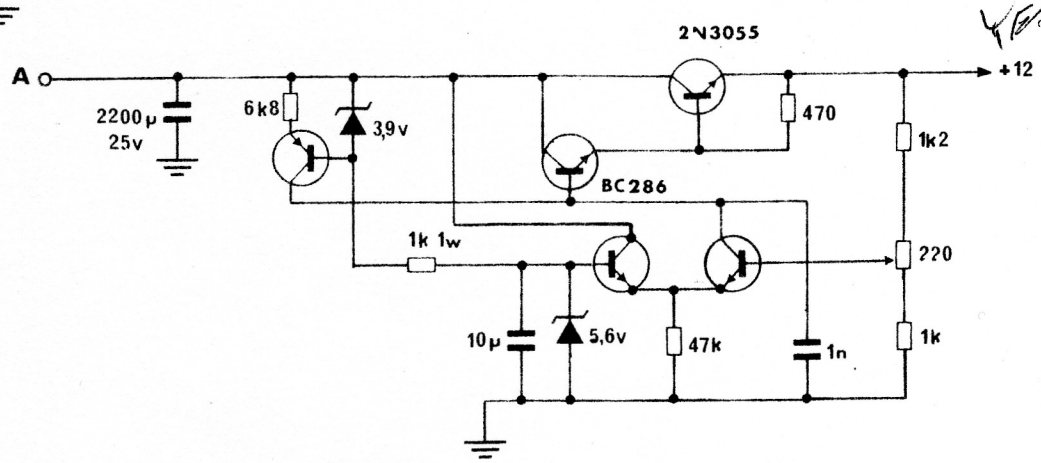
10
11
12
13
14
15
16
17
3k3
25 k
2k2
100µ
470
+12
220
150
22n
10×BC173C
(BC239C)
10µ
25k
ADSR
OSC 3
2k2
47k
100
1k8
10k
100k
-12
18
330
1k
50µ
470 µ
1µ
47k
4×BC173
(BC239)
1k2
220
68k
100
2k2
3,9
30 CA3080
22k
VOL
out HIGH
out LOW
33k
8k2
390
INITIAL VOLUME
+5
1k5
2,2µ
8,2k
1k2
4k7
0,22µ
2,5µ
100k
w
p
20
from DWG C
2 k2
1k
NOISE GENERATOR
Mod.239
4k7
330
3k3
2N5172
16,8M
0,12 µ
0,033µ
240
560
10k
220k
1M
Red Noise
0,15µ
0,5µ
8k2
3×BC173C
(BC239C)
2×BC173C
(BC239C)
from DWG B
DWG-G

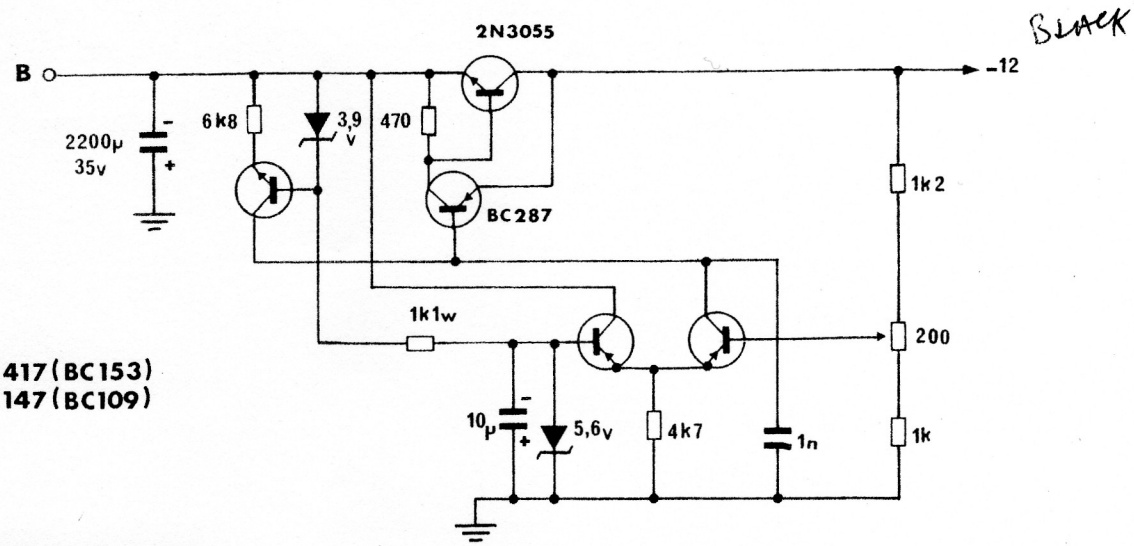
All PNP = BC 417 (BC153)
All NPN = BC 147 (BC109)

Mod. SYNTEX			Serial No			
Nelson	CODE	DRAWN By Dominic Hill	Revision			
		CHECKED By	DATE	21	7	7









All PNP = BC417 (BC153)
All NPN = BC147 (BC109)

POWER SUPPLY Mod.225

Mod.	SYNTEX		SERIAL No			
WELSON	CODE	DRAWN By Dawn	REVISION			
		CHECKED By	DATE	31	7	74

DWG-H

SYNTEX

schematic diagrams

(1974/75)

WELSON
WEBO ELECTRONICS CO. S.p.A.
60020 PASSATEMPO - ITALY

KEYBOARD ENCODER & MEMORY Mod. 216

$\frac{1}{6}$ 7405

-12

3K3 x 37

DO, DO*, RE, RE*, MI, FA, FA*, SOL, SOL*, LA, LA*, SI, DO, DO*, RE, RE*, MI, FA, FA*, SOL, SOL*, LA, LA*, SI, DO, DO*, RE, RE*, MI, FA, FA*, SOL, SOL*, LA, LA*, SI, DO

74151 74151 74151 74151 74151

Vcc

7430

4n7

390

10n

$\frac{1}{3}$ 7410

$\frac{1}{2}$ 7413

680pF

1K 1K

470

29722

2K2 3K3 470pF

74193 74193

74155

74121

33K

2,2µ

3K3

470n

GATE

$\frac{1}{2}$ 7413

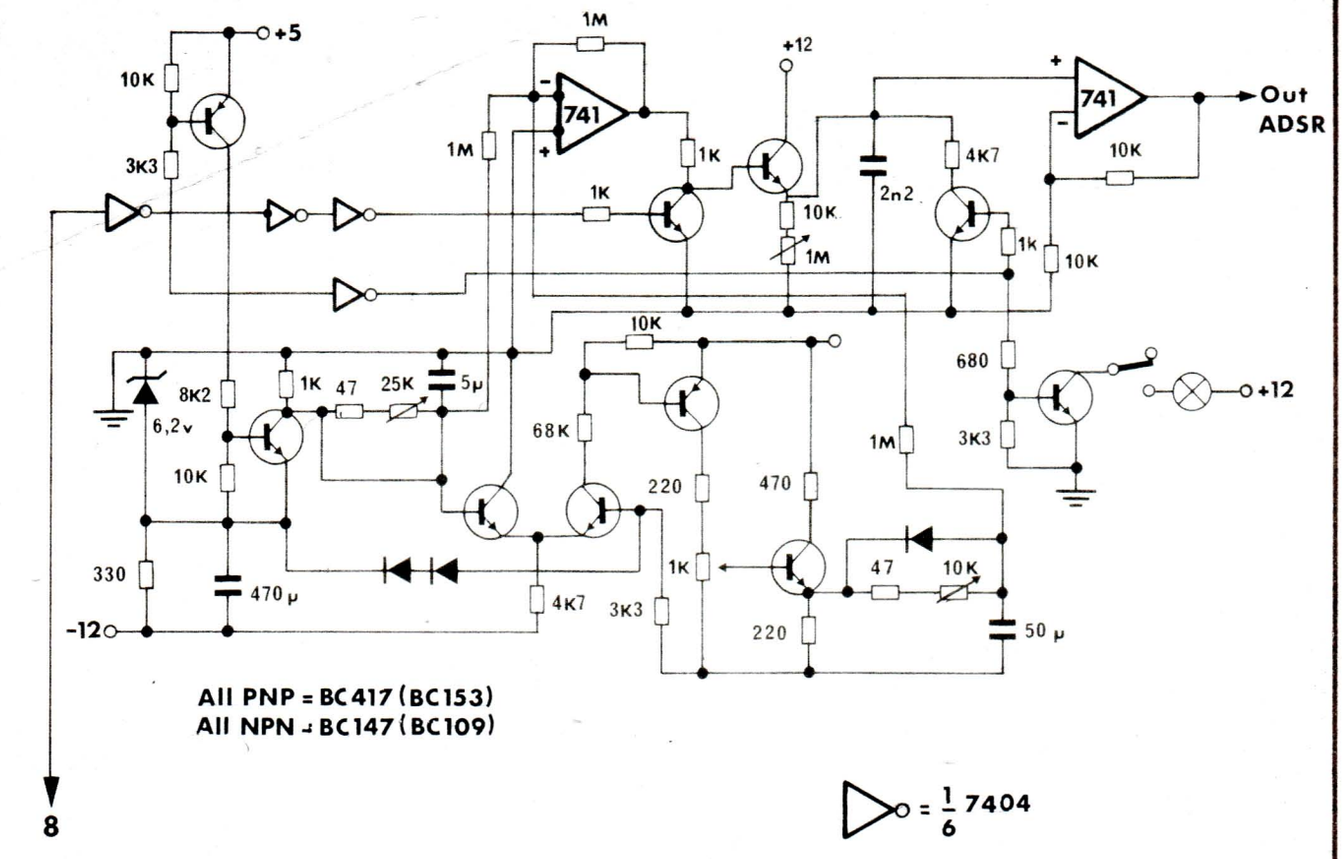
$\frac{1}{3}$ 7410

nc

1 2 3 4 5 6 7

DWG-A

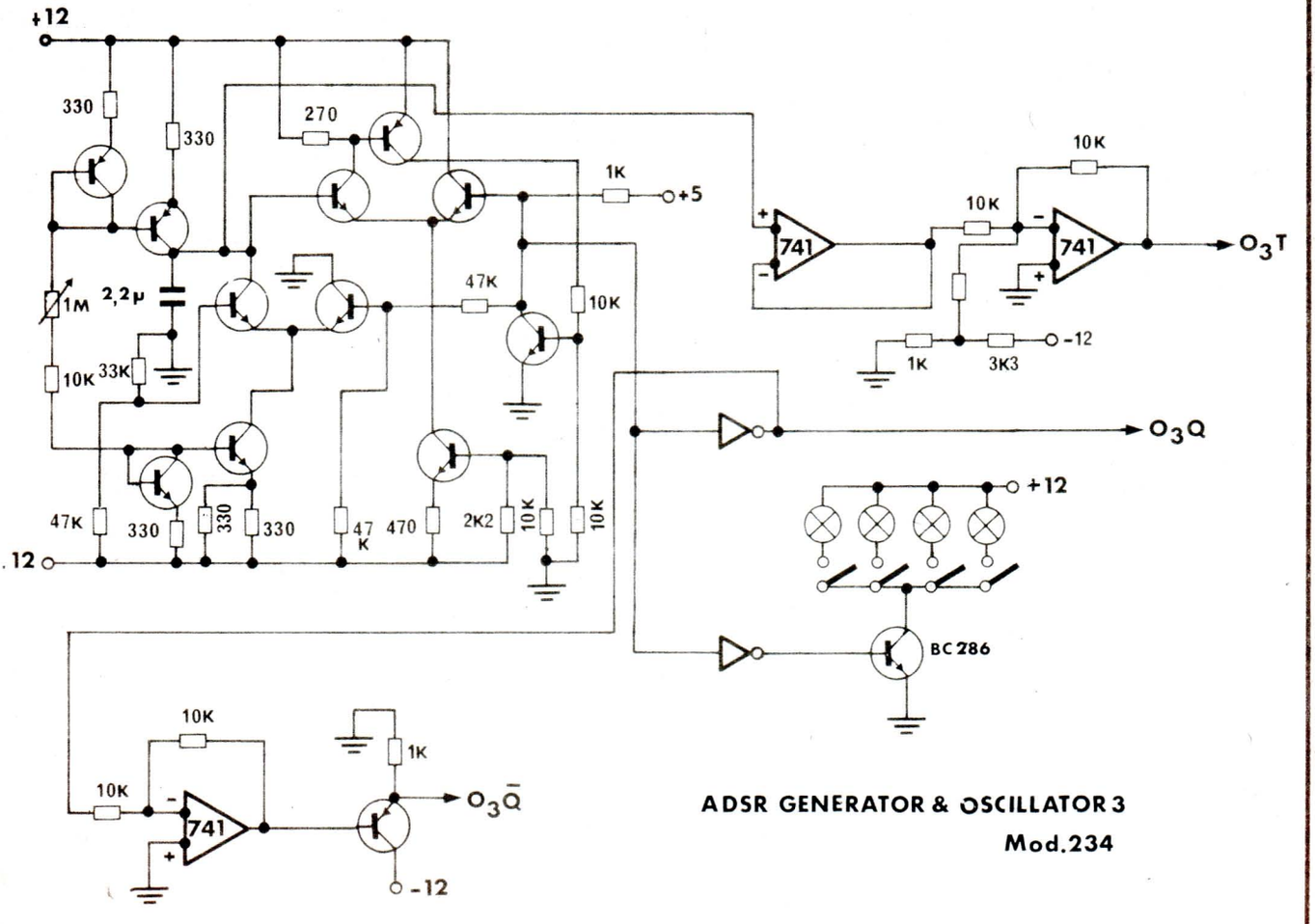
Mod. SYNTEX			SERIAL No			
WELSON	CODE	DRAWN By	REVISION			
		CHECKED By	DATE	31	7	74



All PNP = BC417 (BC153)
All NPN = BC147 (BC109)

8

$\triangleright\!\circ = \frac{1}{6}$ 7404



ADSR GENERATOR & OSCILLATOR 3
Mod.234

Mod.	SYNTEX		SERIAL No			
WELSON	CODE	DRAWN BY Lorin Mitchell	REVISION			
		CHECKED BY S. Mountwell	DATE	31	7	74

DWG-B

CODE CONVERTER 1 MASKED

CODE CONVERTER 2 MASKED

1 2 3 4 5 6 7 8 9

$\frac{1}{2}$ 7451

$\frac{1}{2}$

7472

GLIDE ON OFF

MR

74193 74193 74193

9324 9324 9324

3x7408

Q x12 = BC173C (I.T.T)

741

20 To VCF

O3Q

DZ 3,9v

2x BC417 (BC153)

BC147 (BC109)

$\triangleright$ = $\frac{1}{6}$ 7405

$\sqcap$ = $\frac{1}{4}$ 7400

CODE CONVERTER & CONTROL CIRCUIT

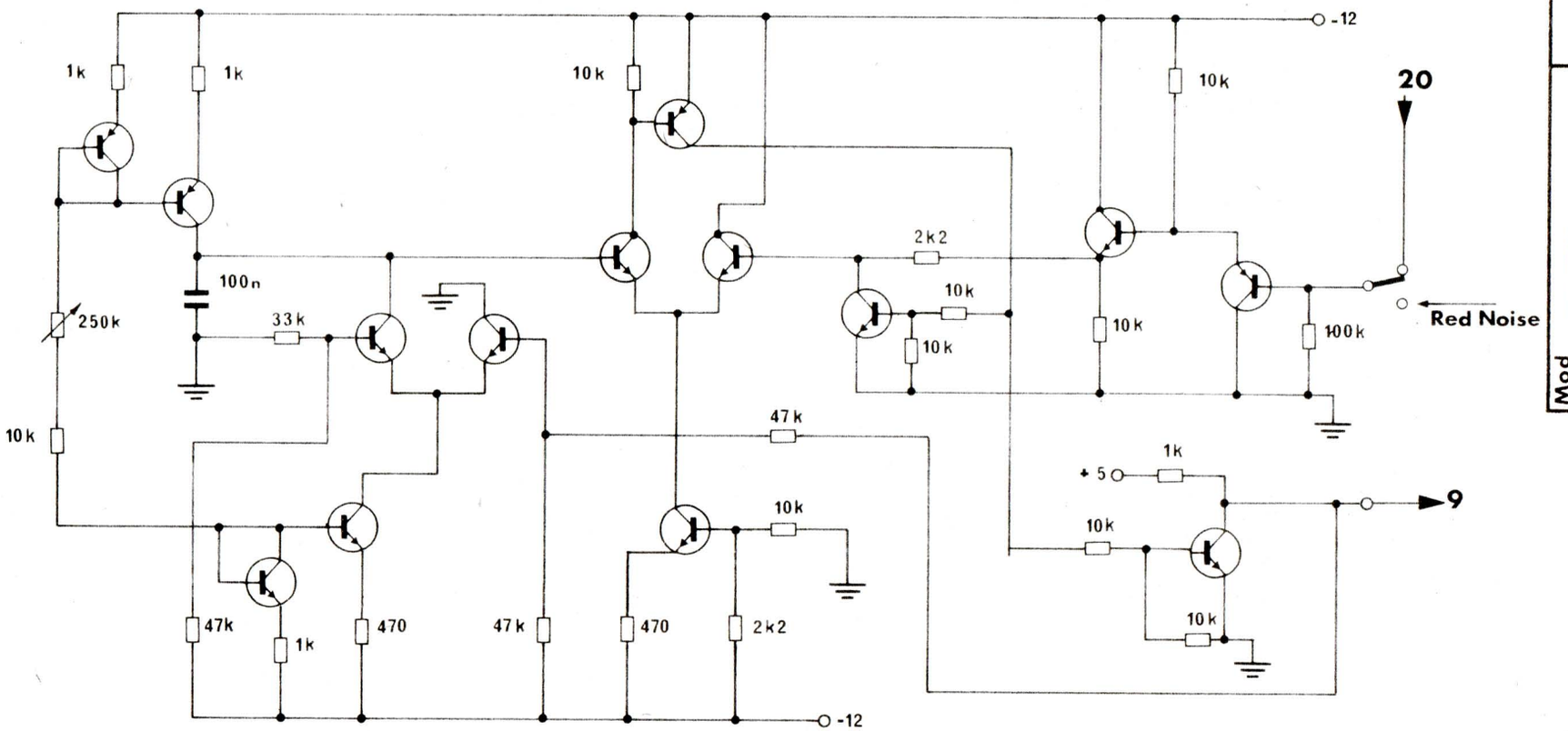
Mod.229

DWG-C

Mod. SYNTEX			SERIAL No			
WELSON	CODE	DRAWN By	REVISION	15	1	75
		CHECKED By S. Mendinall	DATE	31	7	74

PORTAMENTO (GLIDE) OSCILLATOR

Mod.229



All PNP = BC 417 (BC 153)
All NPN = BC 147 (BC 109)

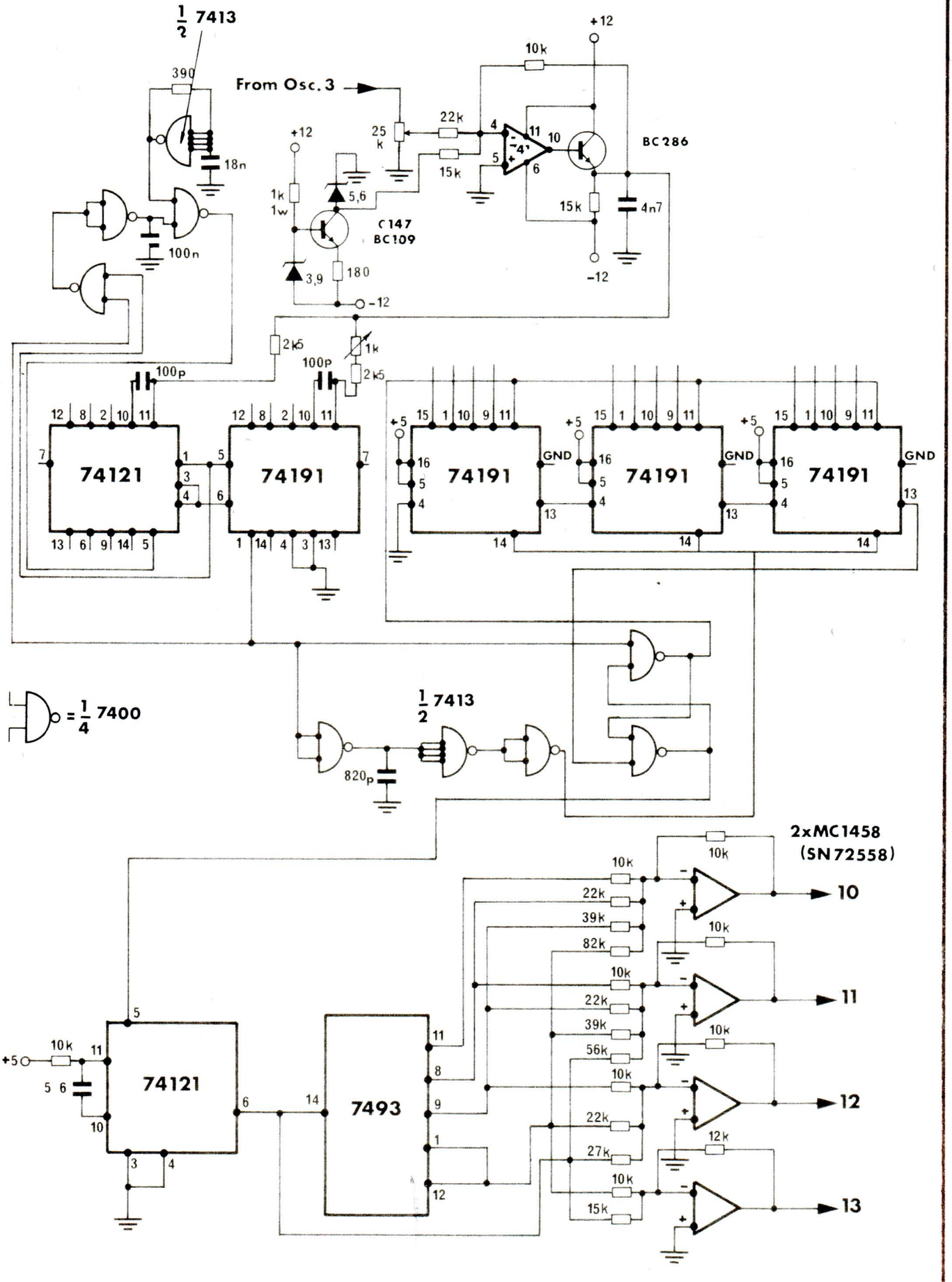
		74
		7
		31
SERIAL No	REVISION	DATE

Mod SYNTEX — DRAWN By — CHECKED By

CODE

WELSON

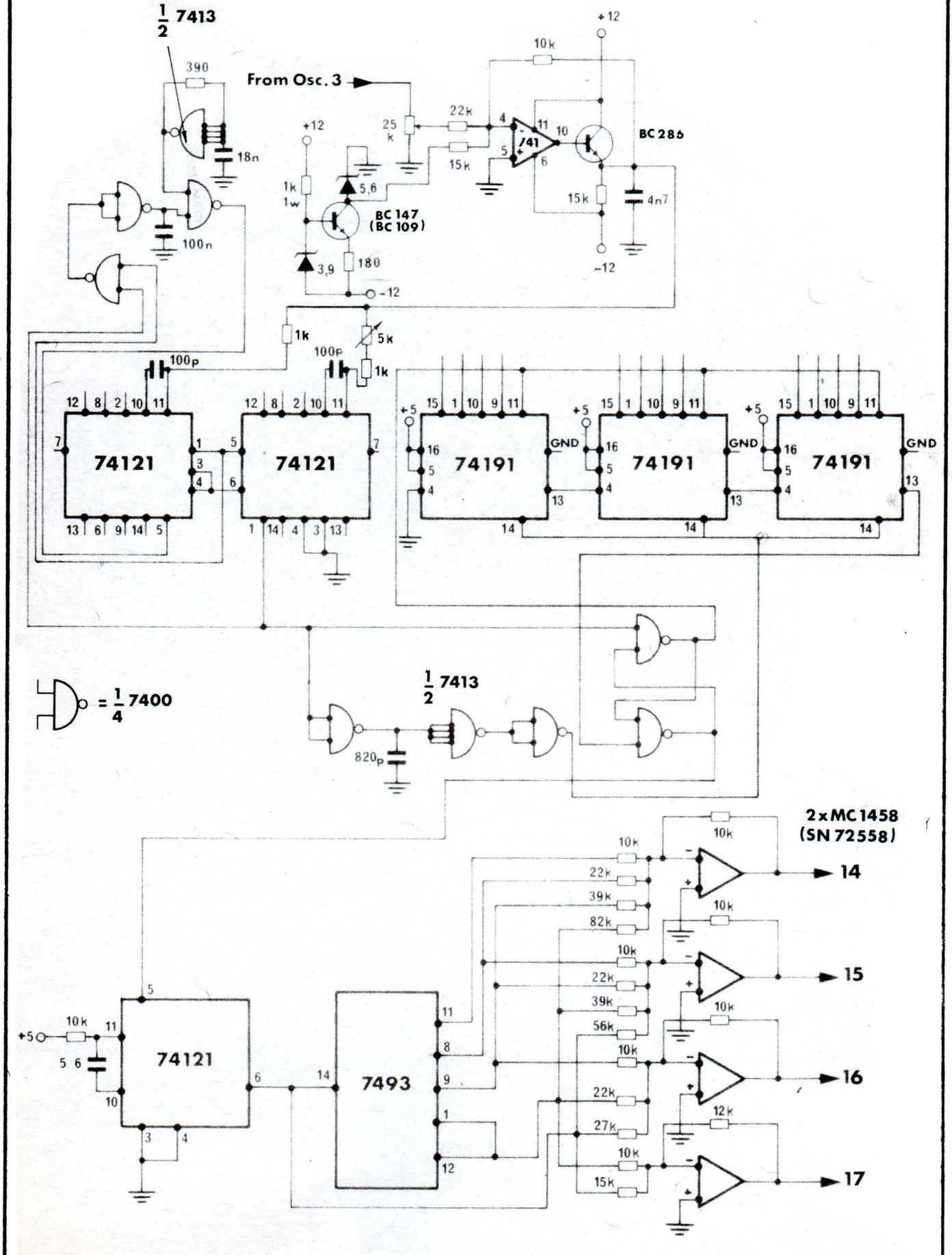
DWG-D



OSCILLATOR 1 Mod.223

DWG-E

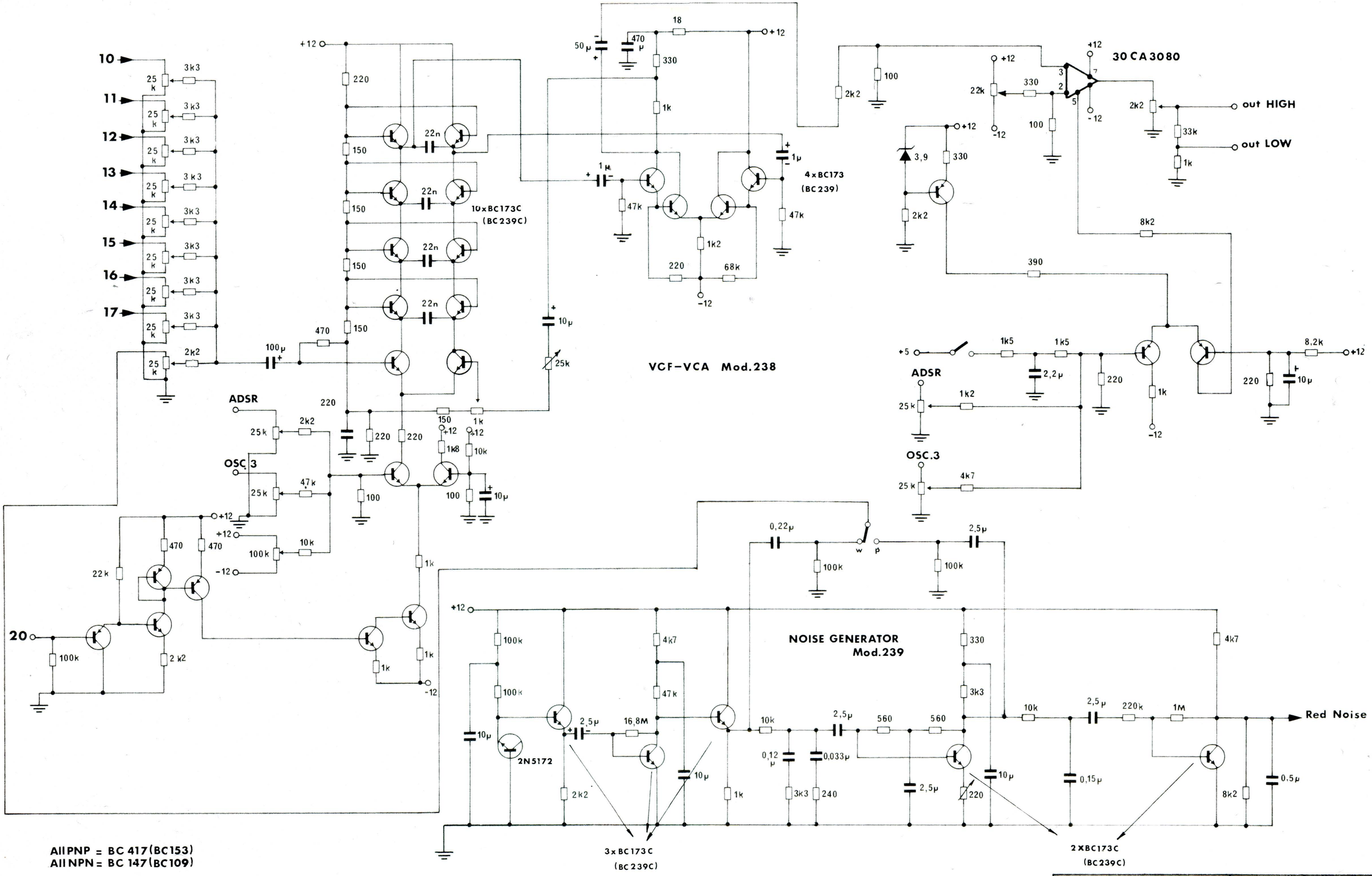
WELSON	Mod. SYNTEX		SERIAL No			
	CODE	DRAWN By	REVISION			
		CHECKED By J. Menchinelli	DATE	31	7	74



OSCILLATOR 2 Mod.223

Mod. SYNTEX			SERIAL No			
WELSON	CODE	DRAWN By	REVISION			
		CHECKED By S. Mansfield	DATE	31	7	74

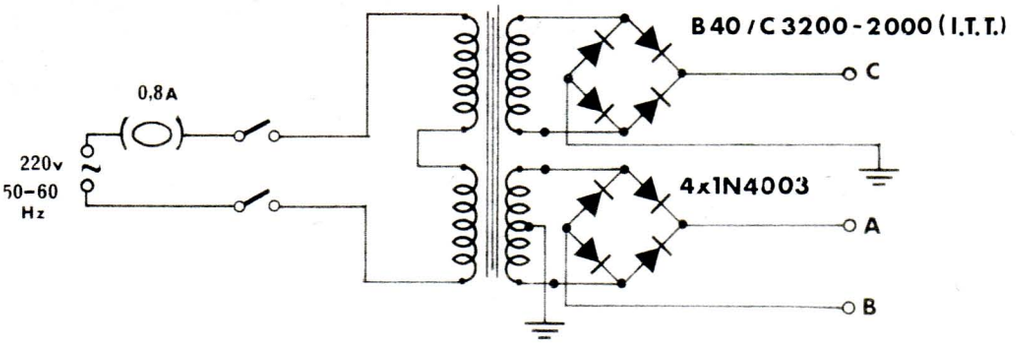
DWG - F

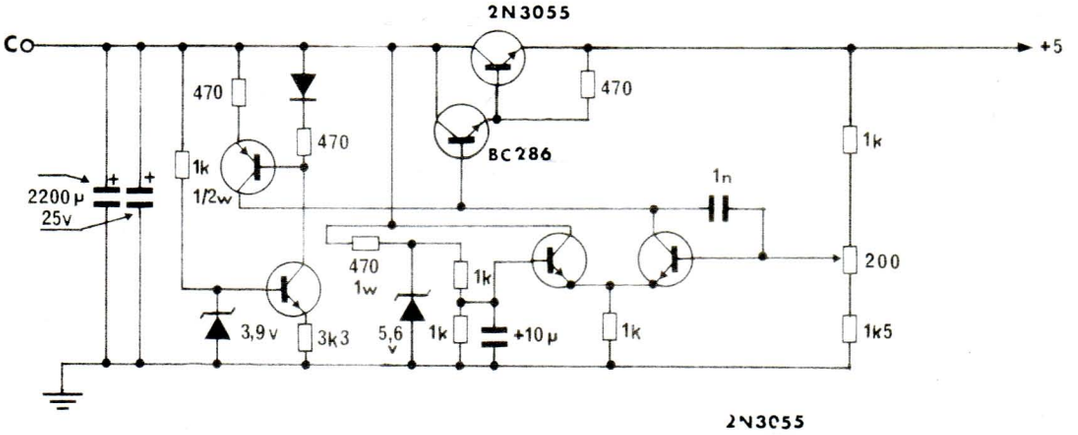


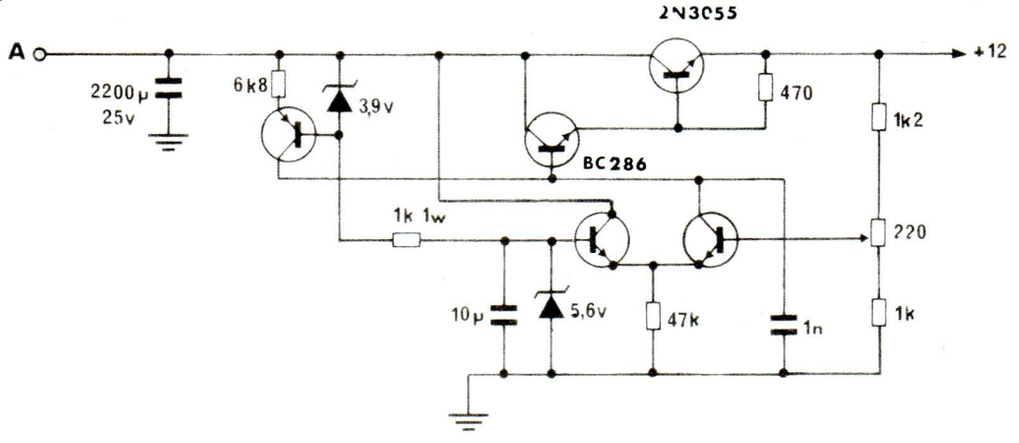
All PNP = BC 417 (BC153)
All NPN = BC 147 (BC109)

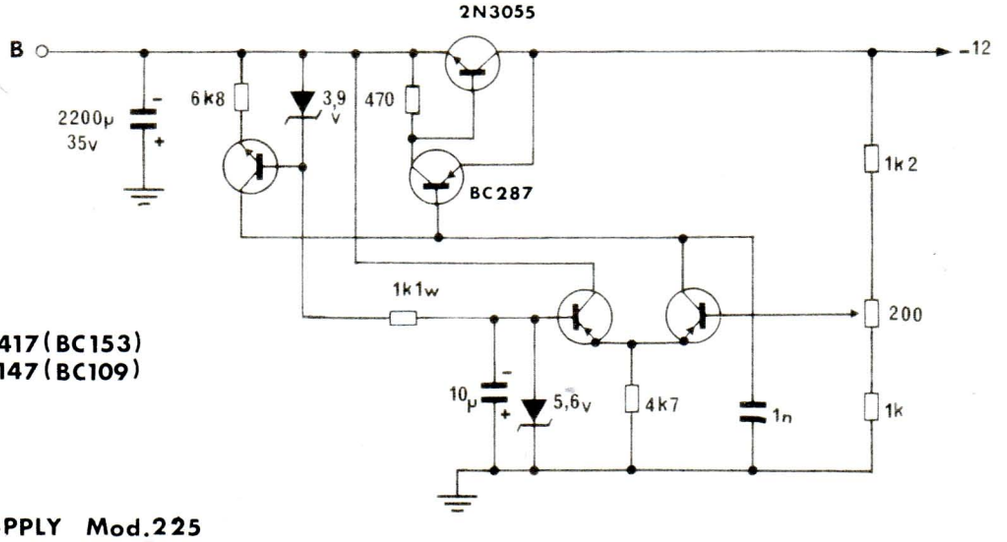
DWG-G

Mod. SYNTEX			Serial No			
Welson	CODE	DRAWN By Domini Mori	Revision			
		CHECKED By S. Mendinelli	DATE	31	7	74









All PNP = BC417 (BC153)
All NPN = BC147 (BC109)

POWER SUPPLY Mod.225

Mod.	SYNTEX		SERIAL No			
WELSON	CODE	DRAWN By Dominic Pilbeam	REVISION			
		CHECKED By S. Hendwell	DATE	31	7	74

DWG-H

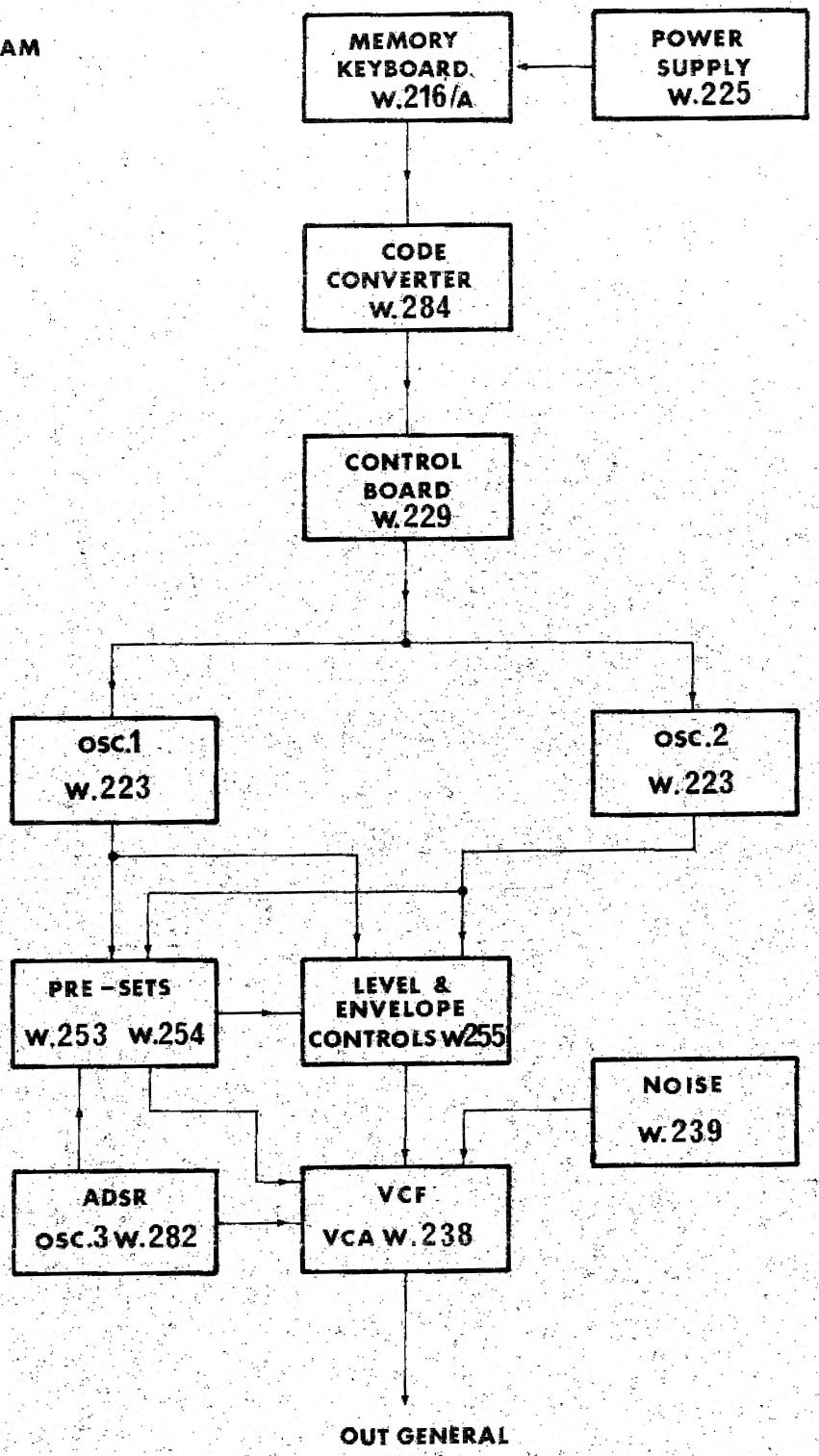
SYNTEX

schematic diagrams

(1976)

WELSON
WEBO ELECTRONICS CO. S.p.A.
60020 PASSATEMPO - ITALY

BLOCK DIAGRAM



Mod. SINTEX			Serial No			
Welson	Code	Drawn By Domenico Mastrolia	Revision	14	6	76
		Checked By Sallechowski	Date			

MEMORY & KEYBOARD W.216/A

C BASS

-12v

3k3 x37

DO, DO*, RE, RE*, MI, FA, FA*, SOL, SOL*, LA, LA*, SI, DO, DO*, RE, RE*, MI, FA, FA*, SOL, SOL*, LA, LA*, SI, DO, DO*, RE, RE*, MI, FA, FA*, SOL, SOL*, LA, LA*, SI, DO

R1 74151

R2 74151

R3 74151

R4 74151

R5 74151

R6 74151

+5v

L1

E1 = 7405
G1 = 7410
H1 = 7413
L1 = 7430
O1 = 7475
O2 = 7475
P1 = 7493
P2 = 7493
Q1 = 74121
R1 = 74151
R2 = 74151
R3 = 74151
R4 = 74151
R5 = 74151
R6 = 74151
S1 = 74155

P1 7493

P2 7493

Q1 74121

O1 7475

O2 7475

S1 74155

VIOLET, BROWN, GRAY, RED, WHITE, ORANGE, PINK, YELLOW

BLACK, GREEN, LIGHT BLUE, BLUE

A Ā B B̄ C C̄ D D̄ E Ē F F̄ G

GRAY To DWG - C

To DWG-B

C SHARP

DWG-A

Mod. SINTEX			Serial No		
WELSON	Code	Drawn By Dawin Lu Rio	Revision	14	6 76
		Checked By Stefano	Date		

TO DWG-C

CODE CONVERTER
W.284

A1 = 7400
A2 = 7400
A3 = 7400
B1 = 7401
B2 = 7401
B3 = 7401
B4 = 7401
B5 = 7401
B6 = 7401
C1 = 7402
D1 = 7404
D2 = 7404
F1 = 7408
G2 = 7410
G3 = 7410
I1 = 7420
M1 = 7451

A B C D E F G H I L M N
RED ORANGE YELLOW GREEN BLUE VIOLET GRAY WHITE PINK BLACK LIGHT BLUE

+5v 3K3

½ 7451

BROWN VIOLET RED GRAY ORANGE WHITE YELLOW PINK

FROM DWG-A

BLACK BLUE

DWG-A

DWG-B

Mod. SINTEX			Serial No		
WELSON	Code	Drawn By	Revision	14	6 76
		Checked By	Date		

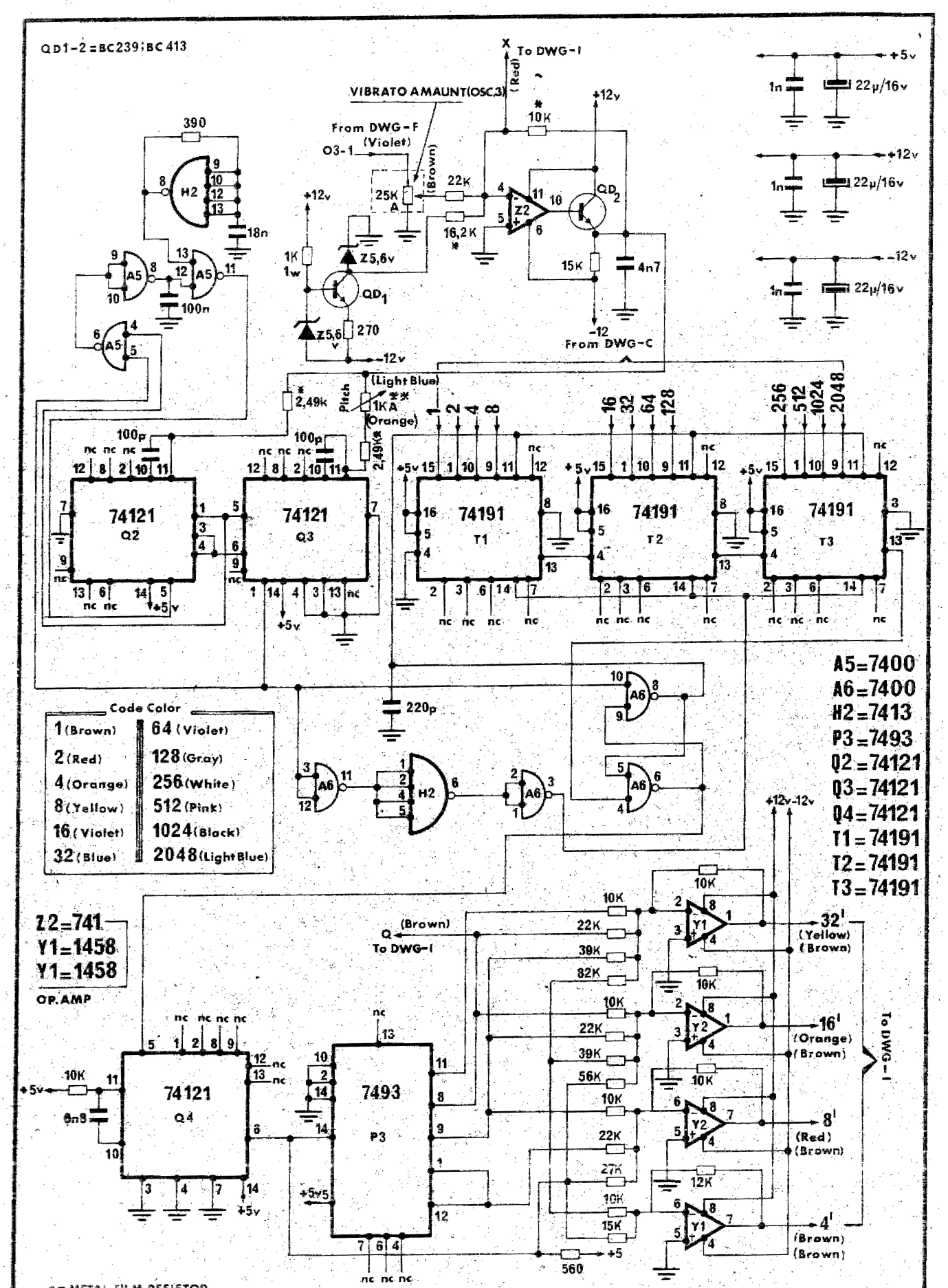
= 7400
= 7405
= 7408
= 7408
= 7408
!= 7451
= 7472
= 74193
= 74193
= 74193
= 9324
= 9324
= 9324

NPN TRANSISTOR ARE BC173 OR BC413
PNP " " BC153 OR BC253

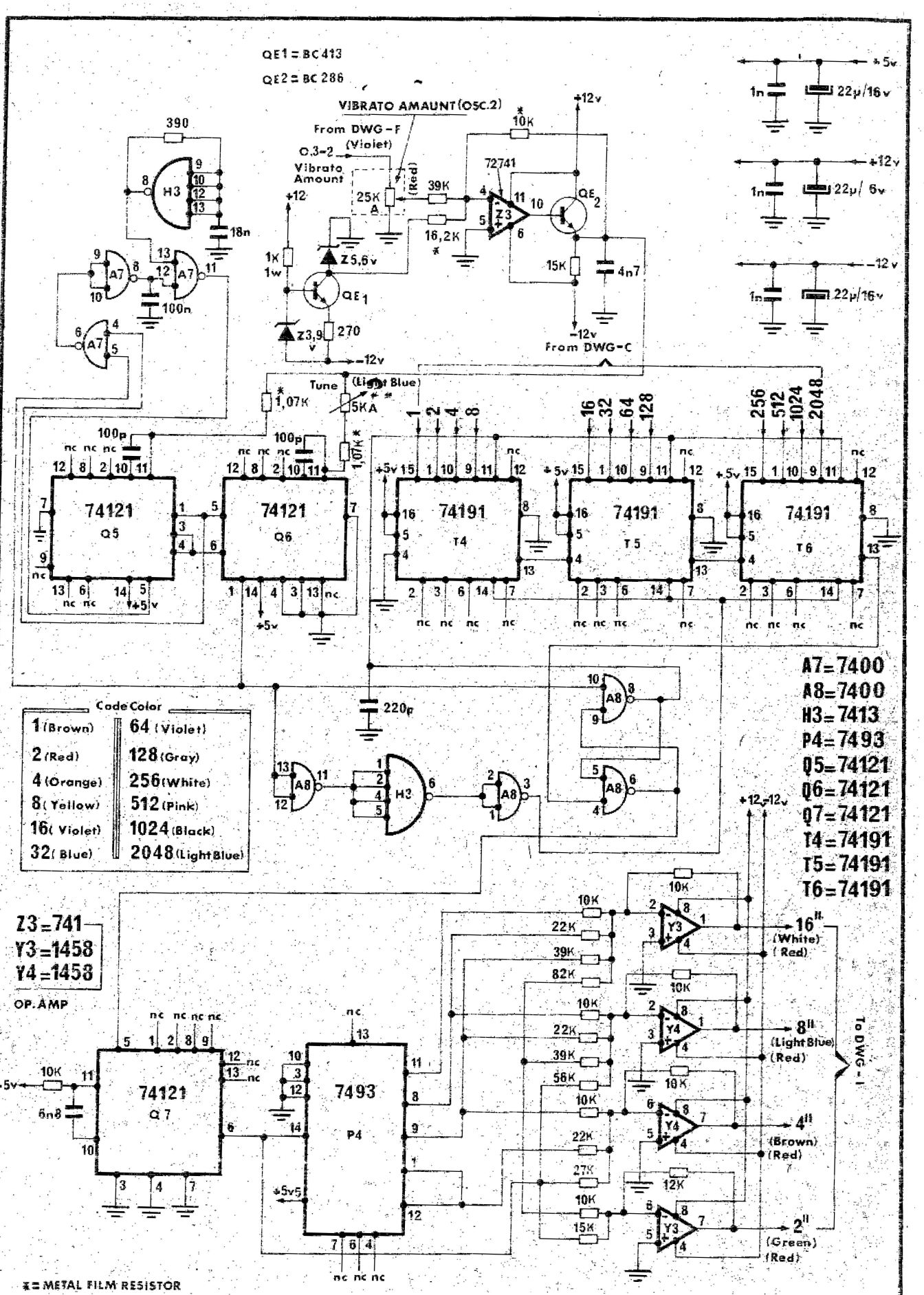
CONTROL BOARD W.229

DWG-C

Mod. SINTEX			Serial No			
	Code	Drawn By Dario M. Pitt	Revision	14	6	76
		Checked By	Date			



Mod. SINTEX			Serial No		
Wilson	Code	Drawn By Dawin M. Rita	Revision	14	6 76
		Checked By	Date		



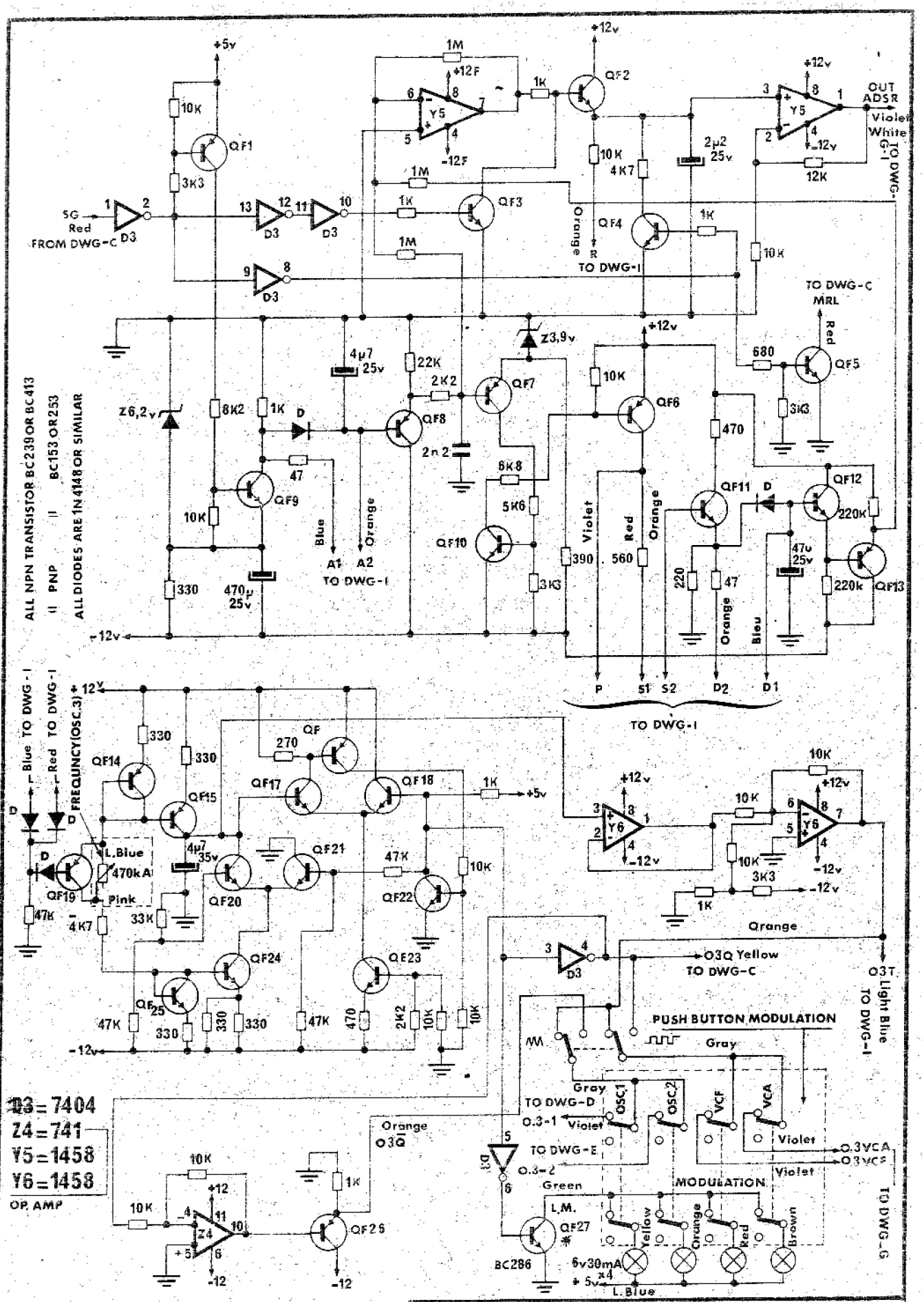
* = METAL FILM RESISTOR

* * WIRE WOUND POTENTIOMETER

Oscillator 2 W. 223

DWG-E

Mod. SINTEX			Serial No		
Wilson	Code	Drawn By: Dario M. Rita	Revision	14	6 76
		Checked By:	Date		

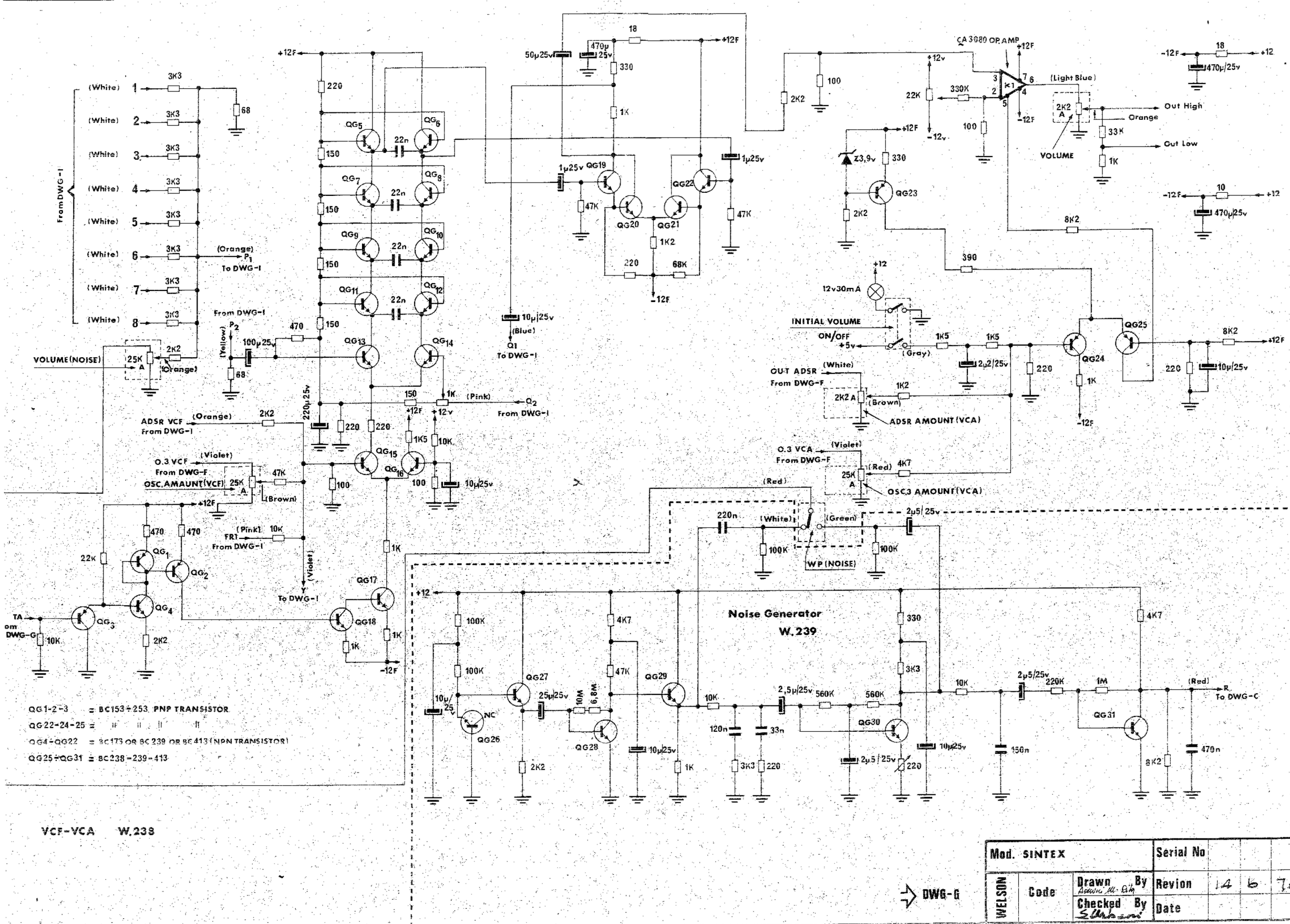


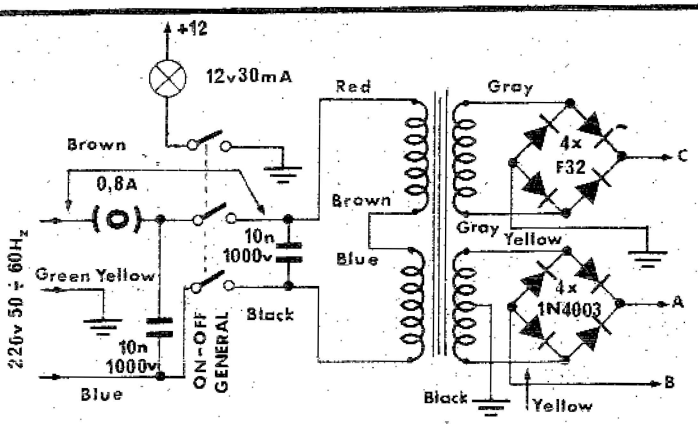
ADSR-OSC.3

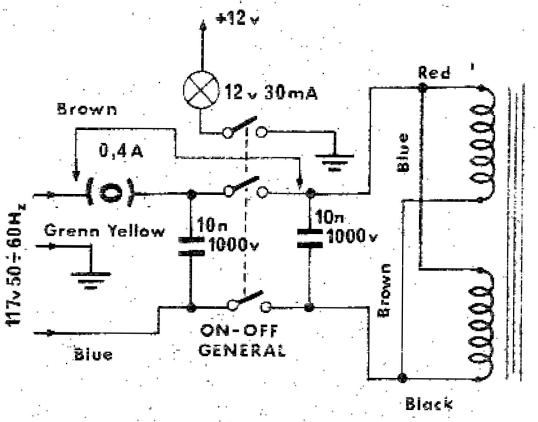
W.282

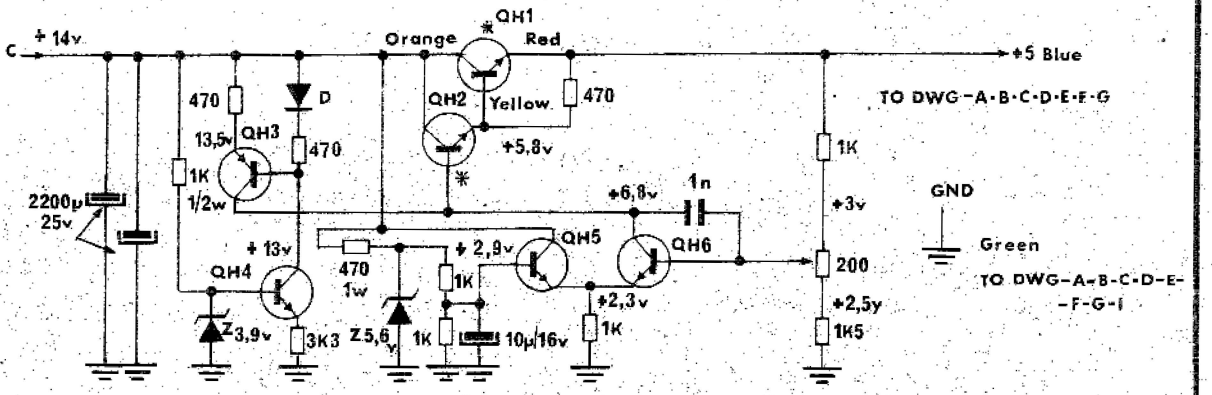
DWG -F

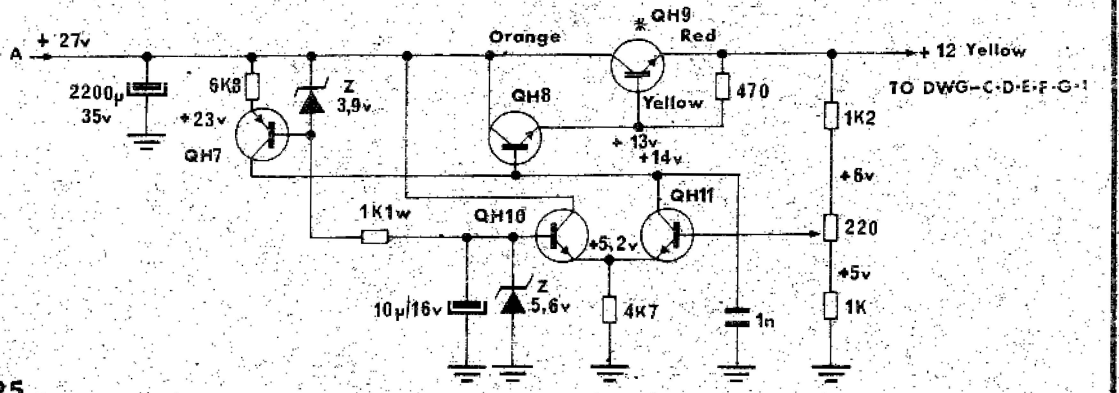
Welson	Code	Mod. SINTEX		Serial No	
		Drawn By Domin M-Rte		Revision	14 6 76
		Checked By Stefano		Date	


From DWG-I
(White) 1 3K3
(White) 2 3K3
(White) 3 3K3
(White) 4 3K3
(White) 5 3K3
(White) 6 3K3
(White) 7 3K3
(White) 8 3K3
68
(Orange) P1 To DWG-I
VOLUME (NOISE)
25K A
2K2
(Orange)
From DWG-I P2
(Yellow)
100µ25v
470
68
ADSR VCF From DWG-I
(Orange)
2K2
220µ25v
220
220
150
+12F
+12v
1K
(Pink)
Q2 From DWG-I
1K5
10K
10µ/25v
O.3 VCF From DWG-F
(Violet)
OSC.AMAUNT(VCF)
25K A
47K
(Brown)
100
FRT From DWG-I
(Pink)
10K
470
470
22K
QG1
QG2
QG3
QG4
TA om DWG-G
10K
2K2
(Violet) Y To DWG-I
QG17
QG18
1K
1K
-12F
50µ25v
470µ 25v
18
330
1K
1µ25v
QG19
47K
QG20
QG21
QG22
1K2
220
68K
1µ25v
47K
-12F
10µ/25v
(Blue) Q1 To DWG-I
2K2
100
CA 3080 OP.AMP
+12v
-12v
22K
330K
K1
(Light Blue)
2K2 A
Out High
Orange
33K
Out Low
1K
VOLUME
Z3,9v
330
QG23
2K2
8K2
390
12v30mA
INITIAL VOLUME
ON/OFF
+5v
(Gray)
1K5
1K5
2µ2/25v
220
QG24
QG25
1K
8K2
220
10µ/25v
OUT ADSR From DWG-F
(White)
2K2 A
(Brown)
1K2
ADSR AMOUNT (VCA)
O.3 VCA From DWG-F
(Violet)
(Red) 4K7
25K A
OSC.3 AMOUNT (VCA)
(Red)
220n
(White)
100K
(Green)
WP (NOISE)
2µ5/25v
100K
Noise Generator
W.239
100K
100K
10µ/25
NC
QG26
QG27
25µ/25v
10M
6,8M
QG28
2K2
4K7
47K
QG29
10µ/25v
1K
10K
120n
33n
3K3
220
2,5µ/25v
560K
560K
QG30
2µ5/25v
220
330
3K3
10µ/25v
10K
2µ5/25v
220K
1M
QG31
150n
8K2
470n
4K7
(Red) R To DWG-C
QG1-2-3 = BC153÷253 PNP TRANSISTOR
QG22-24-25 = " " " "
QG4÷QG22 = BC173 OR BC 239 OR BC 413 (NPN TRANSISTOR)
QG25÷QG31 = BC238-239-413
VCF-VCA W.238
DWG-G
Mod. SINTEX
Serial No
WELSON
Code
Drawn By
Checked By
Revion 14 6 76
Date

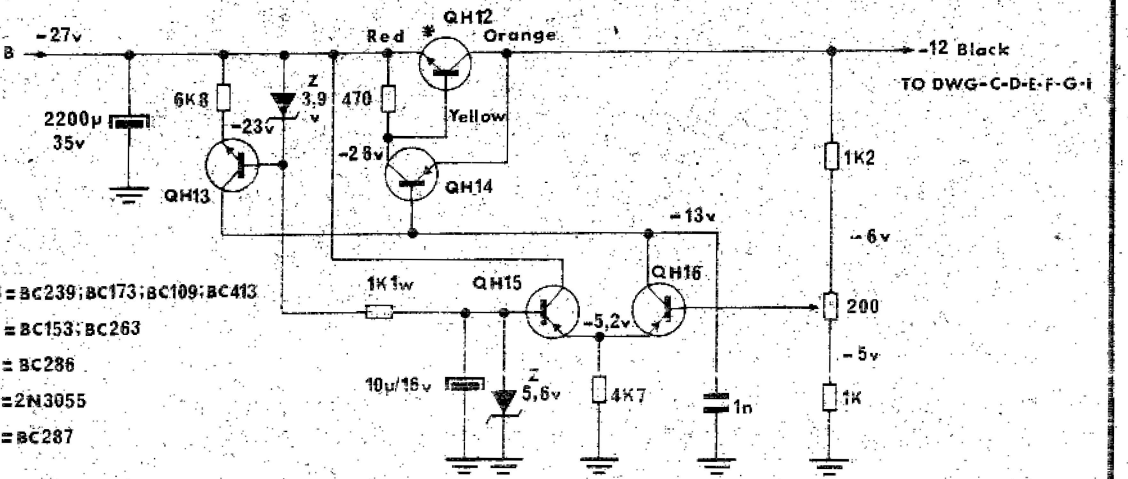








W. 225



QH4-5-6-10-11-13 = BC239; BC173; BC109; BC413
QH3-7-15-16 = BC153; BC263
QH2-8 = BC286
QH1-9-12 = 2N3055
QH14 = BC287

* TRANSISTOR ON METAL HEAT SINK

POWER SUPPLY

DWG -H

Welson	Code	Mod. SINTEX		Serial No		
		Drawn By Gianni M. Rizzi		Revision	14	6 76
		Checked By Siviero		Date		

1 Flute
2 Trombone
3 Horn
4 Oboe
5 Bass Clarinet
6 Jan Harp
7 Wha-Wha
8 Accordion
9 Strings
10 Xylophone
11 Bass Guitar
12 Spinet
13 Space
14 Fuzz
15 Musical Saw

PRE-SETS CIRCUIT

W.253 W.254

470K 10K 470K +12 From DWG-F L

22K 22K 1K (Red)

50K 330K 1K 100K 180K 470K 270K (Red)

RL From DWG-C (Ligh/Blue)

1K (Gray) 4K7 (Gray)

220 +12v 1K 1K/1w → 12v

(White) (Red)

5 6 7 22K 8 9 10 11 12 13 14 4K7 15

4K7 4K7

6k8 6k8 22k 22k 22k 22k 68 6k8 6k8 68 6K8 6K8 6K8 15K 68 18K 18K 68 15K 15K 15K 15K 68 6K8

(White) (Light Blue) (Brown) (Green)
16" 8" 14" 2"
From DWG-E

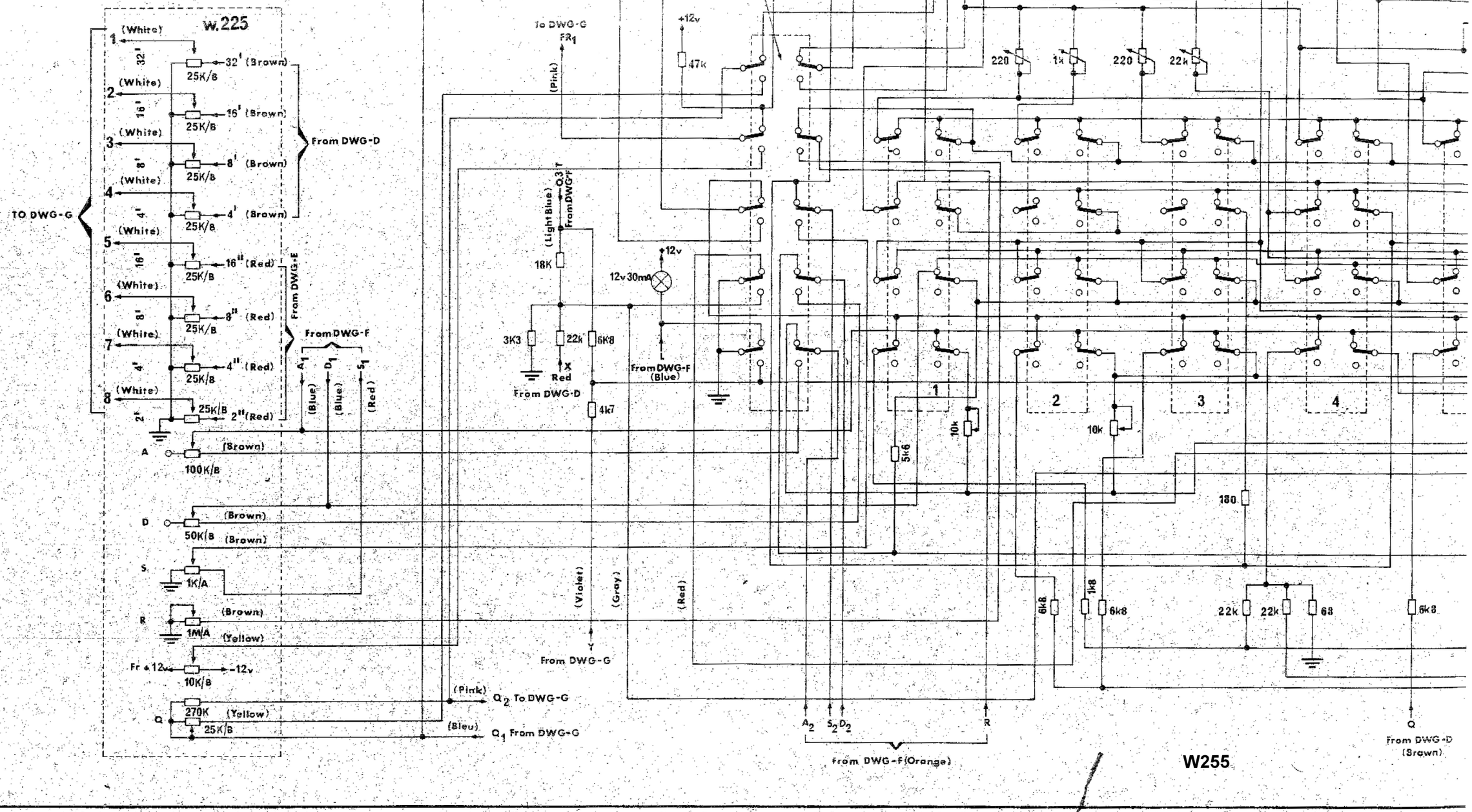
(Yellow) (Orange) (Red) (Brown)
32" 16" 8" 4"
From DWG-D

DWG-I

DWG-D rawn)

Mod. SINTEX			Serial No			
WELSON	Code	Drawn By Dennis W. Welson	Revision	14	6	76
		Checked By Welson	Date			

SLIDER POTENTIOMETER BOARD



W255